Breaking Limits: Terabit Speeds on a single CPU server

Marco Chiesa

KTH Royal Institute of Technology

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Joint work with

Tommaso Caiazzi

Mariano Scazzariello

Hamid Ghasemirahni

Alireza Farshin

Dejan Kostić

Gerald Q. Maguire Jr

Internet Traffic is Growing in Speed and Size

Massive amount of data to be processed at **cloud/edge networks**

External internet-facing

- users, sensors, services
- **terabits** per second (Tbps)
- **millions** of connections per second

Internal machine-to-machine

– big-data, AI/ML, etc

– **thousands** of servers

– **petabits** per second (Pbps) of traffic

Processing massive amounts of traffic at **high rates** is **hard**!

Processing Massive Amounts of Traffic at High Rates is Hard!

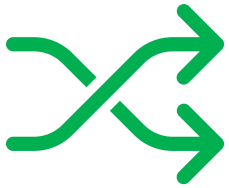
Network Functions Virtualization is an **essential** architectural paradigm of today's data centers

Processing Massive Amounts of Traffic at High Rates is Hard!

Network Functions Virtualization is an **essential** architectural paradigm of today's data centers

NFs are deployed on commodity hardware rather than specialized one

Cost-Effective



Flexible

Scalable

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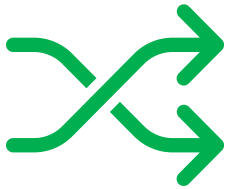


Flexible

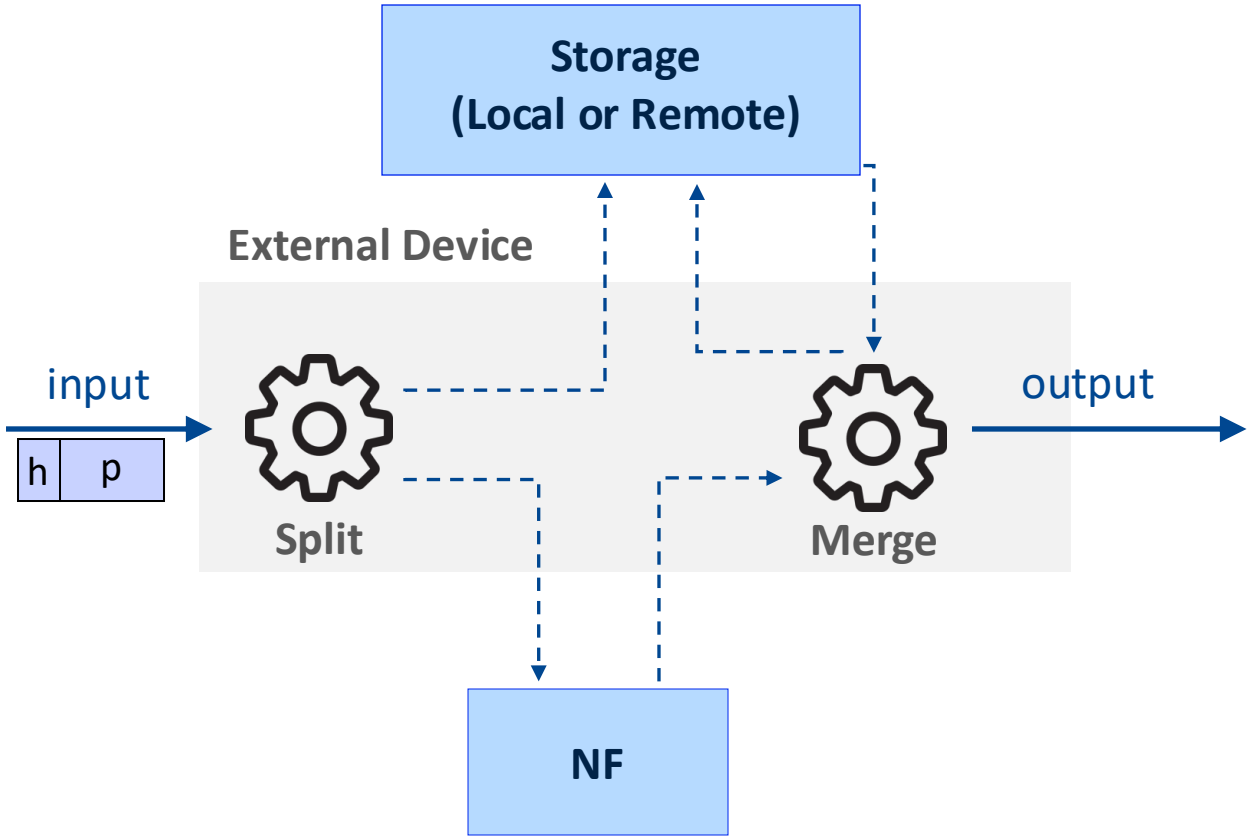
Scalable

Lower performance compared to specialized hardware

Minimize CPU Cycles per Packet

State-of-the-art **packet-splitting** solutions **increase** shallow NFs throughput

e.g., Ribosome, nicmem



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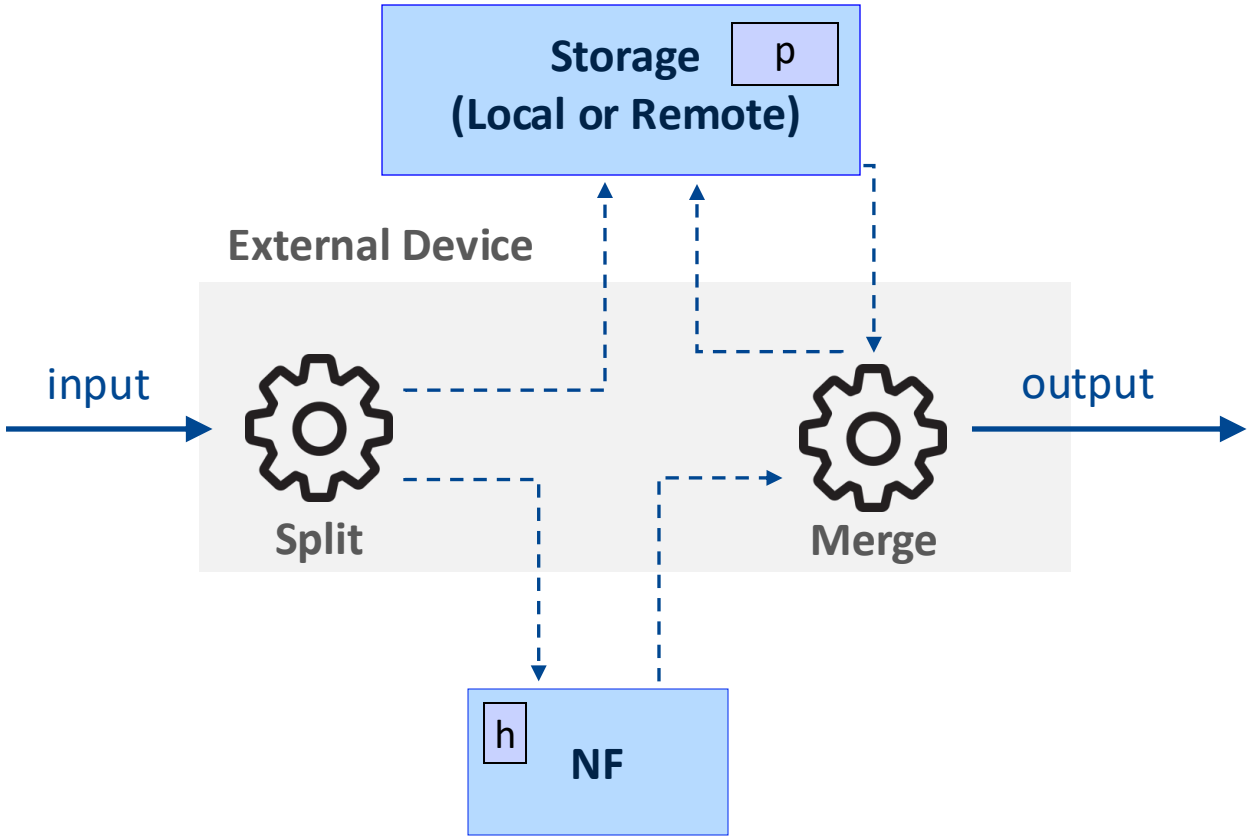

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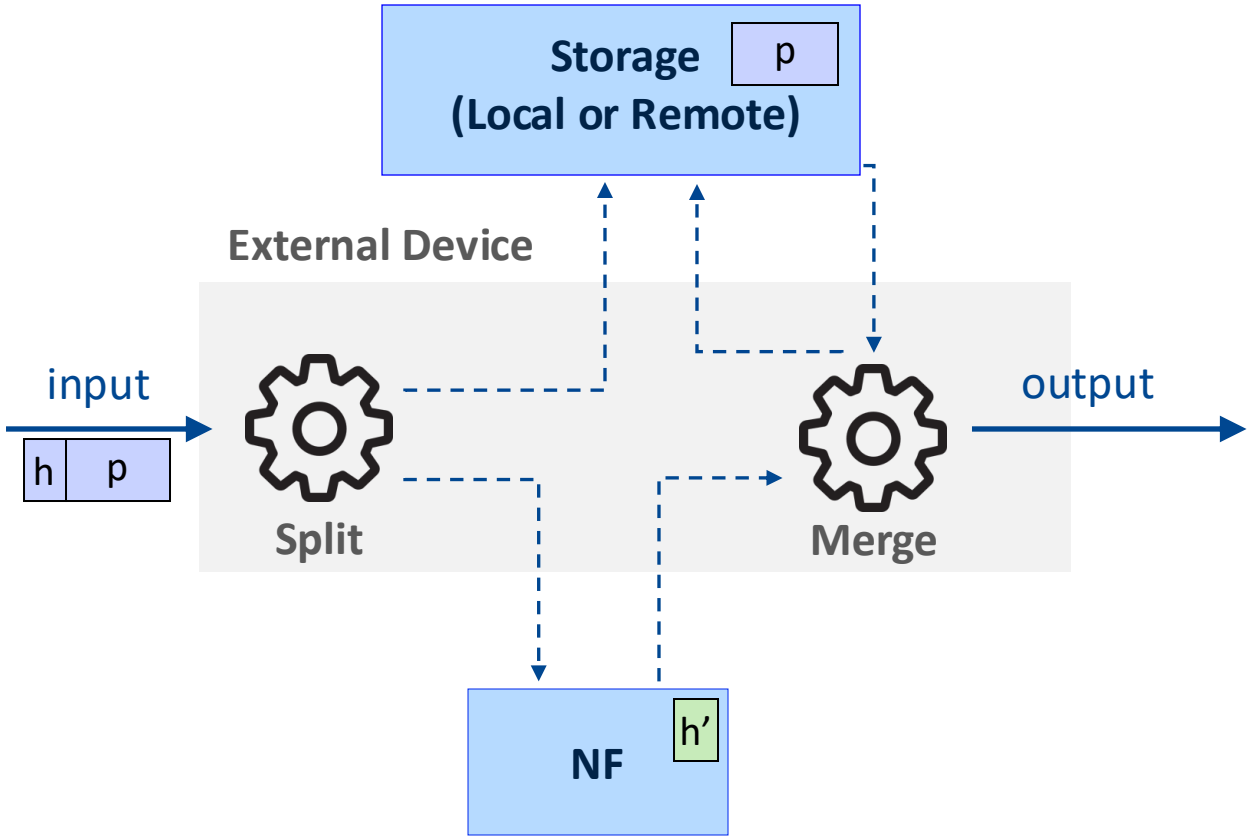

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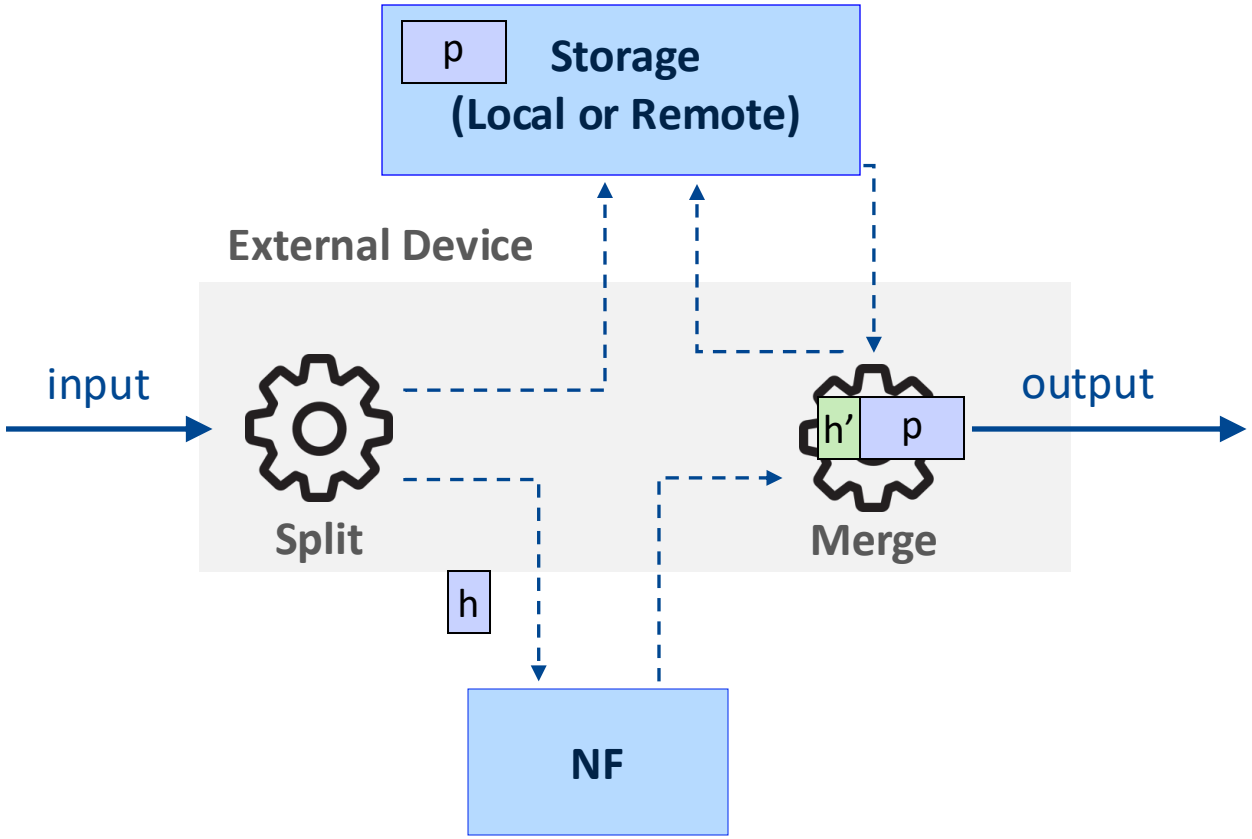

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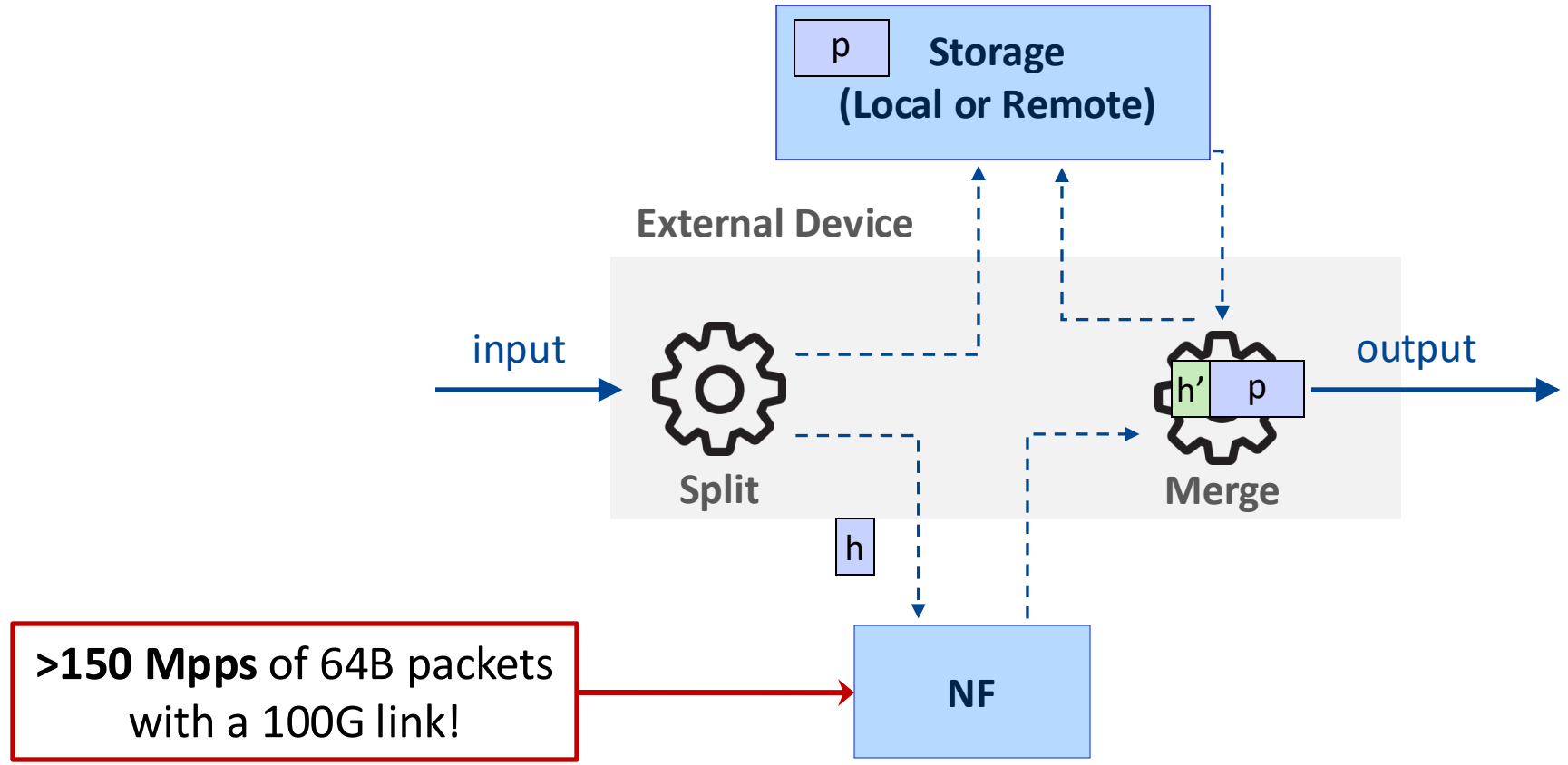

>150 Mpps of 64B packets with a 100G link!

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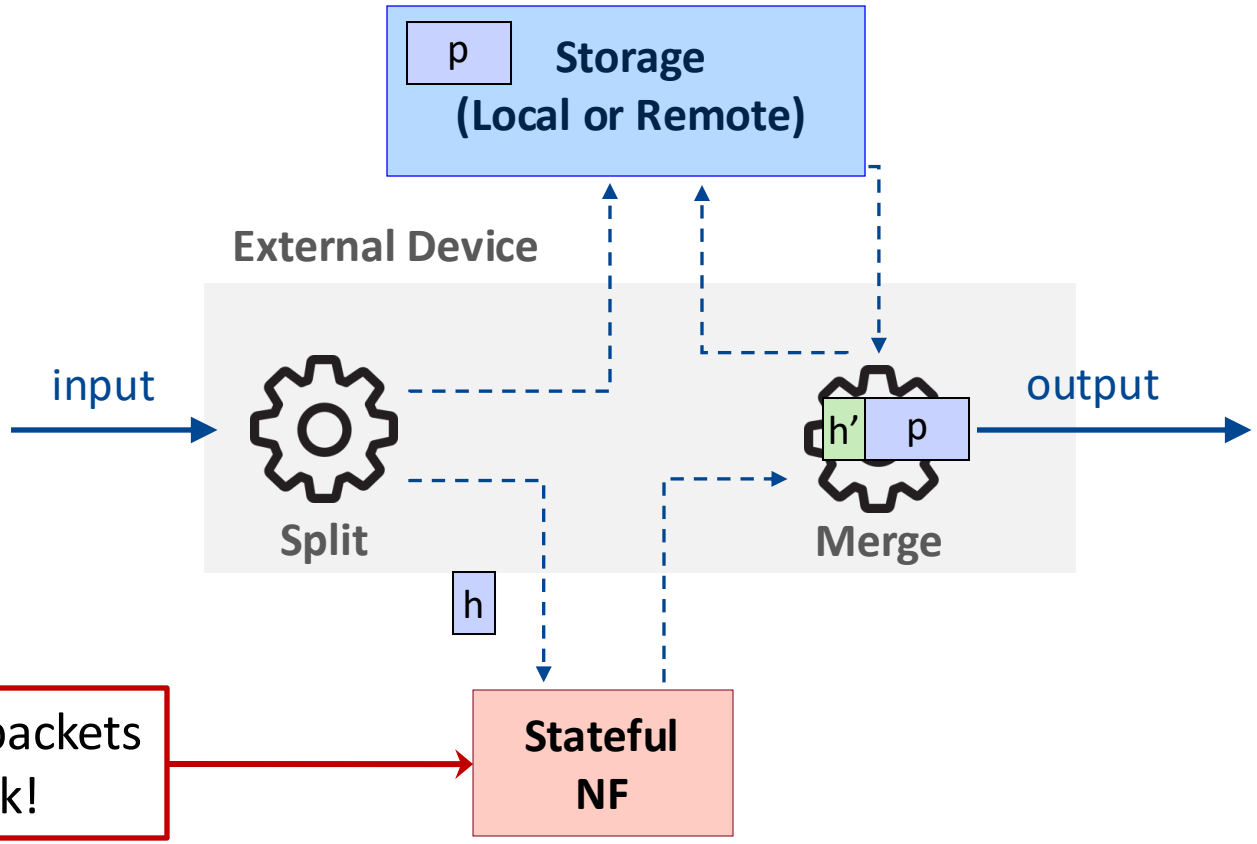

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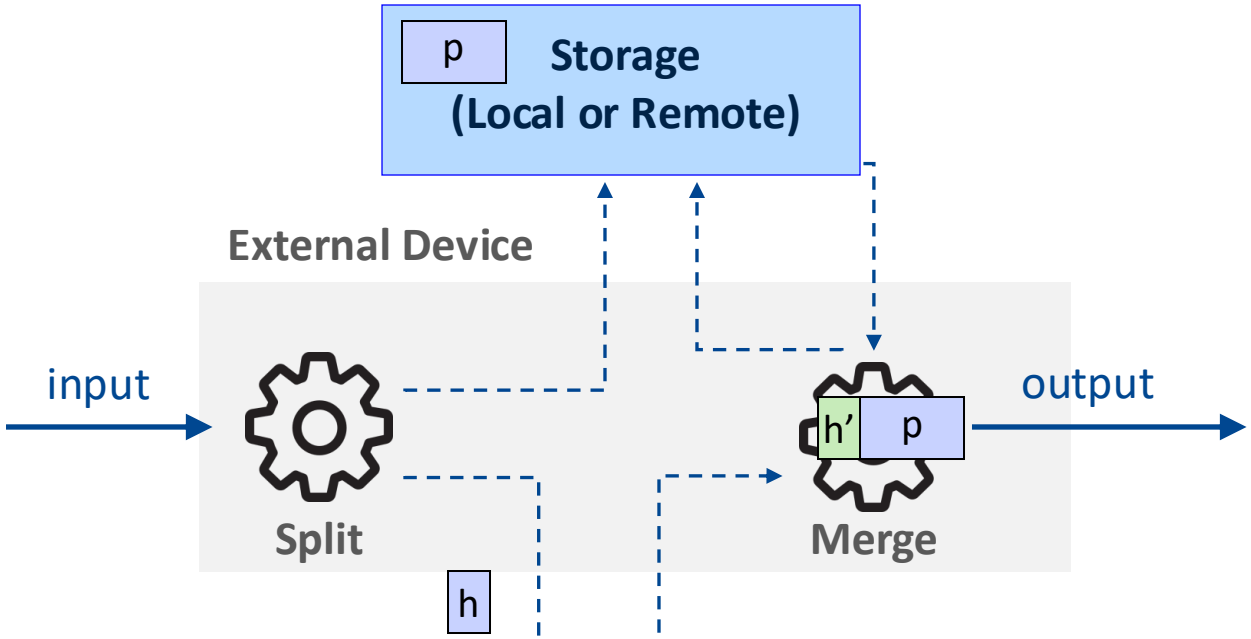
Store **per-flow** states!

Minimize CPU Cycles per Packet

State-of-the-art **packet-splitting** solutions **increase** shallow NFs throughput

None of the existing frameworks can handle such loads!



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Store **per-flow** states**!**

Can we scale complex, stateful
packet processing chains on commodity hardware to
over 100 millions packets per second?

Essential Principles of Stateful Packet Processors

Batch Processing

Minimize Memory Accesses

Minimize Sync. Overheads

Essential Principles of Stateful Packet Processors

- **Batch Processing**

Minimize Memory Accesses

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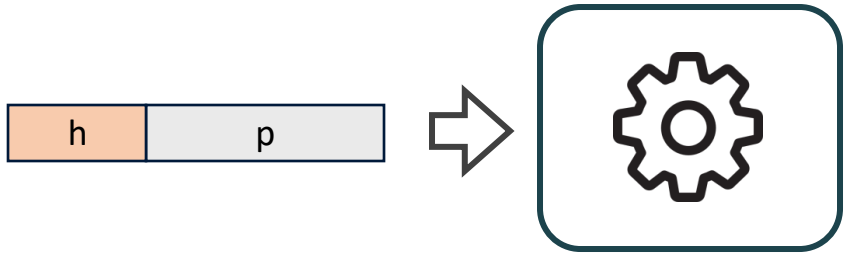


Essential Principles of Stateful Packet Processors

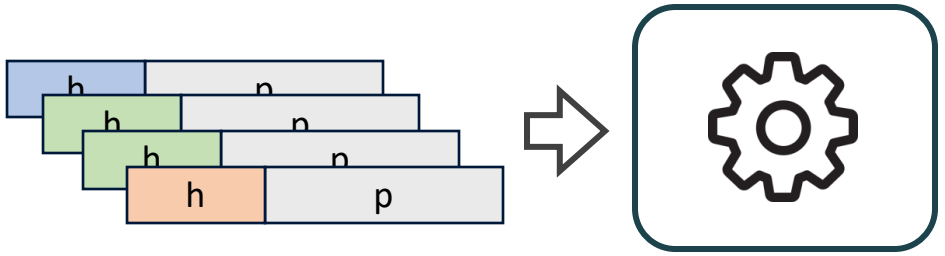
✓ VPP

› Batch Processing

Minimize Memory Accesses

Minimize Sync. Overheads

Process **batches** of packets



Maximizes instruction **cache hits**

Enables **software prefetching** of data

Essential Principles of Stateful Packet Processors

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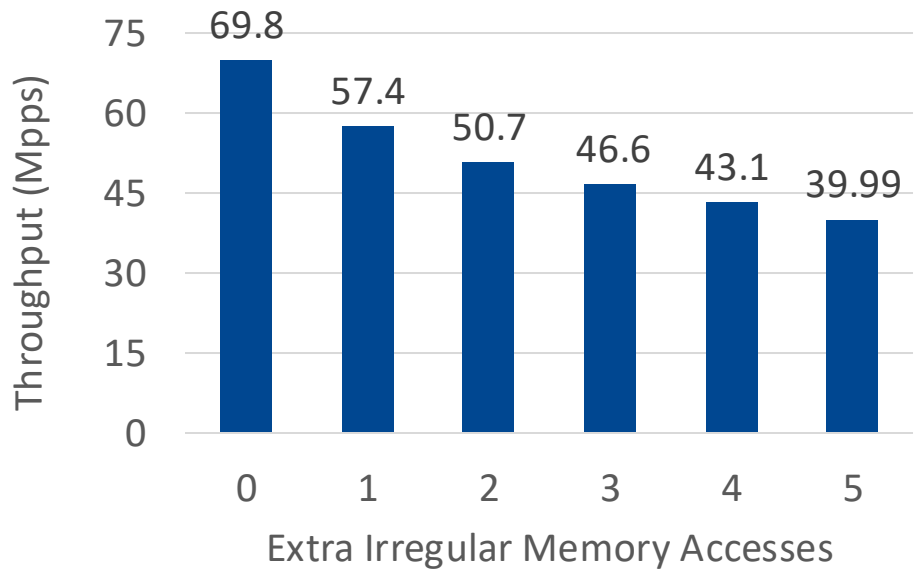
Batch Processing > **Minimize Memory Accesses** **Minimize Sync. Overheads**

Hash tables are the essential data structure in stateful NFs

Require **at least two** random memory accesses



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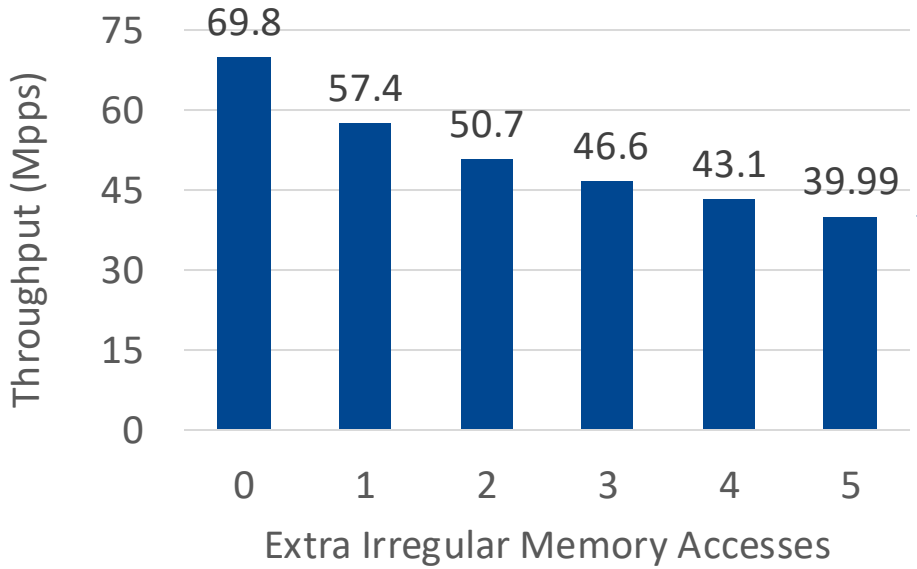


Each memory access **drops performance**!

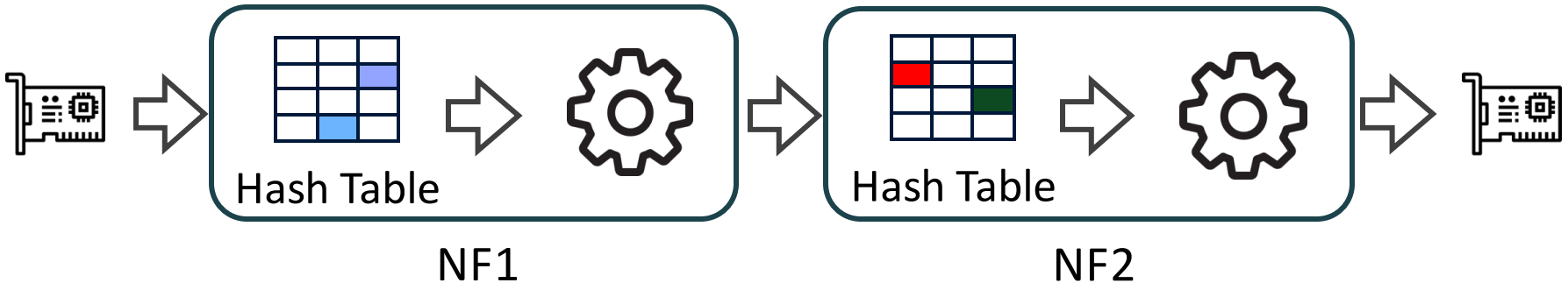
How to **minimize** memory accesses?

Essential Principles of Stateful Packet Processors

✓ VPP

Batch Processing > **Minimize Memory Accesses** **Minimize Sync. Overheads**

? How to **minimize** memory accesses? → **Aggregate** States



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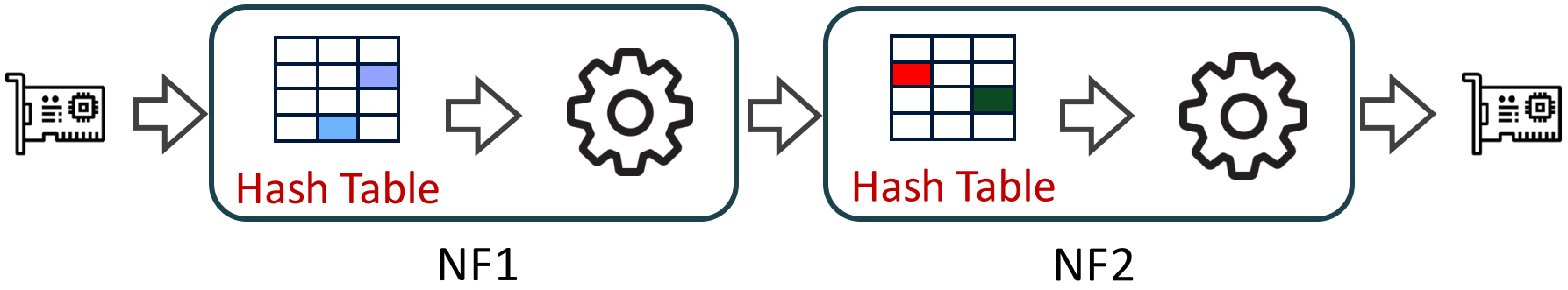

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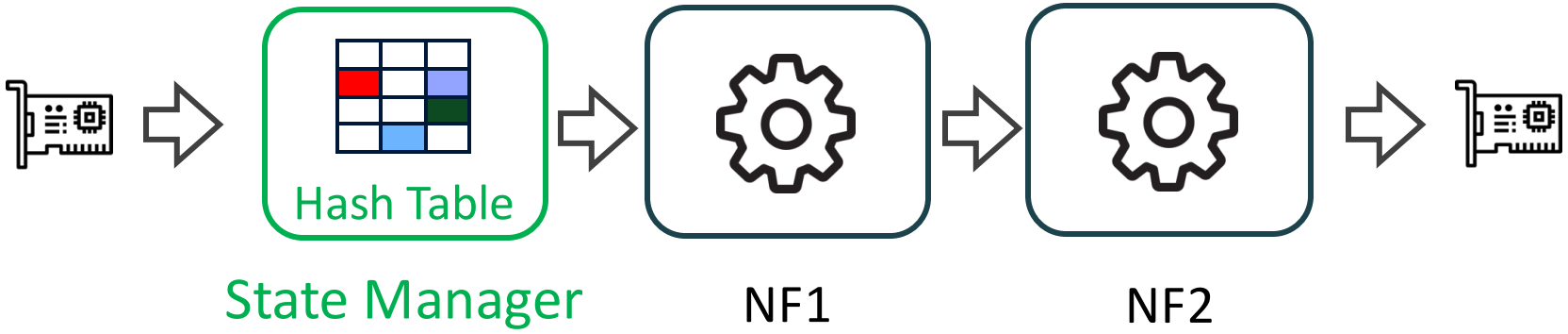

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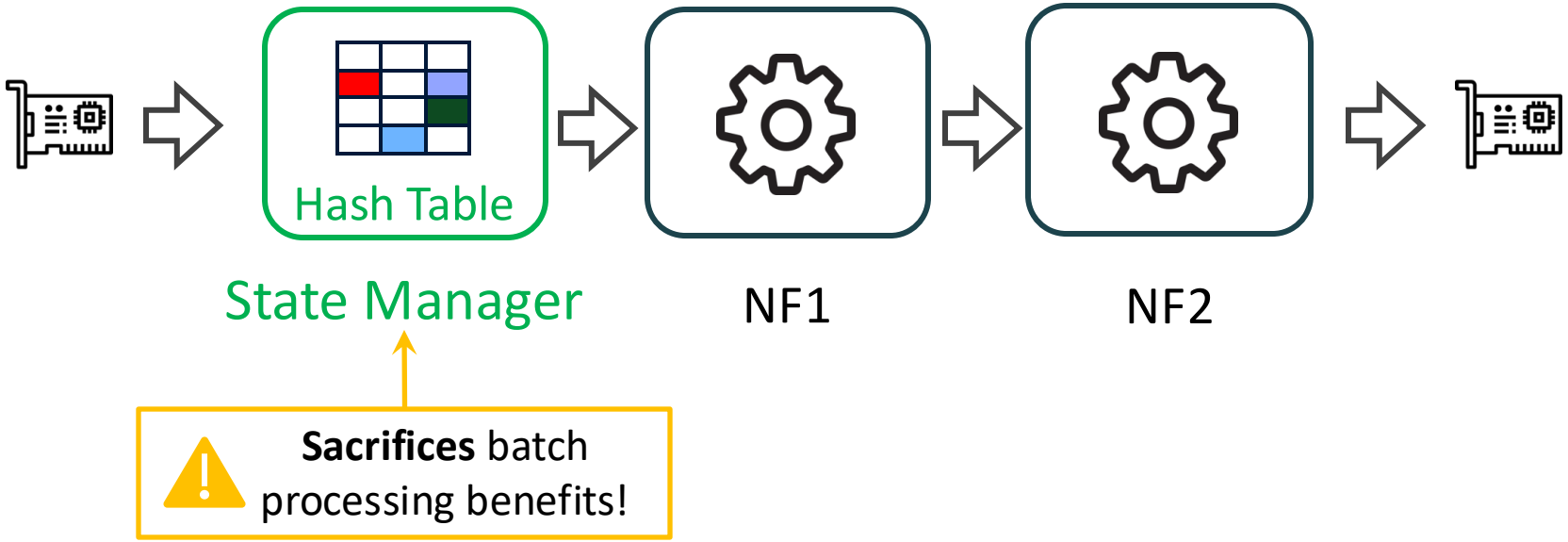

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✓ VPP — **Batch Processing**

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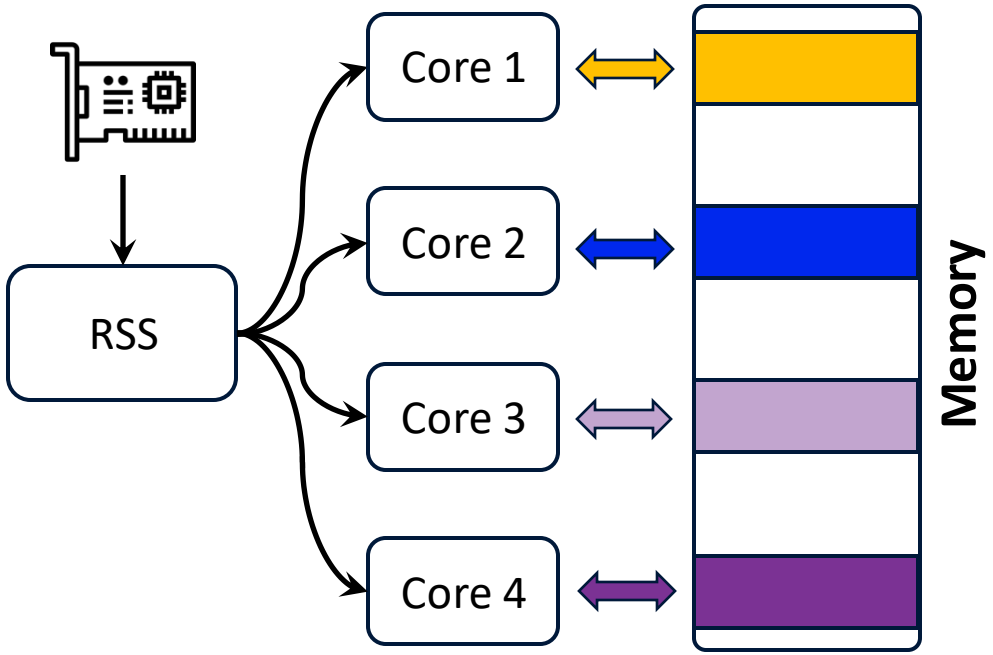
› **Minimize Sync. Overheads**

? How to **scale** NFs on **multiple cores**? ➡ **Shared-Nothing** Model



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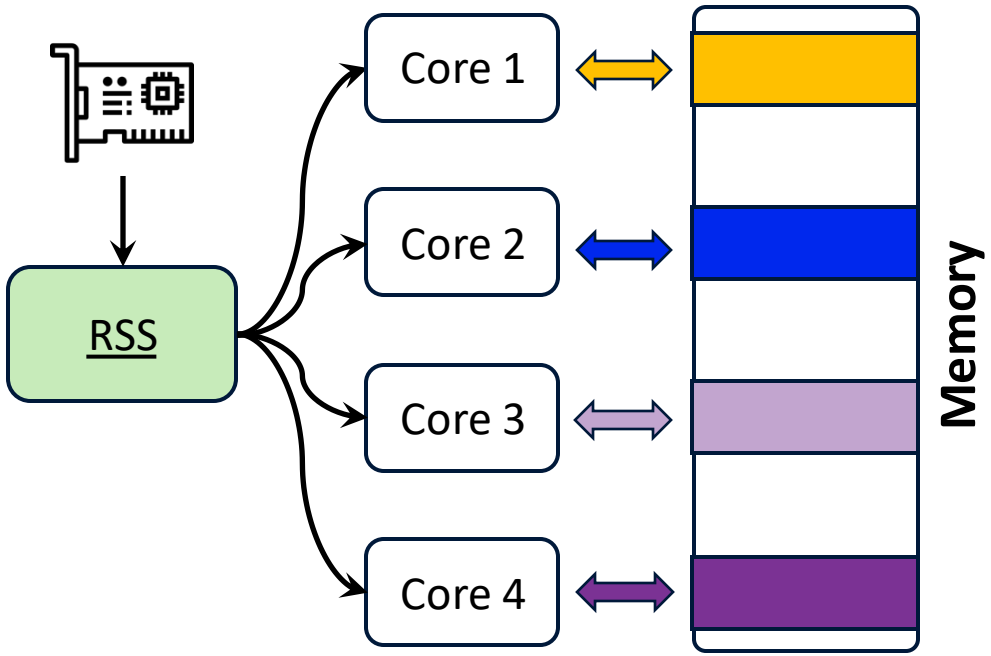
👍 **High Performance**

👍 **Per-flow Consistency**

✗ **Not applicable in all scenarios!**



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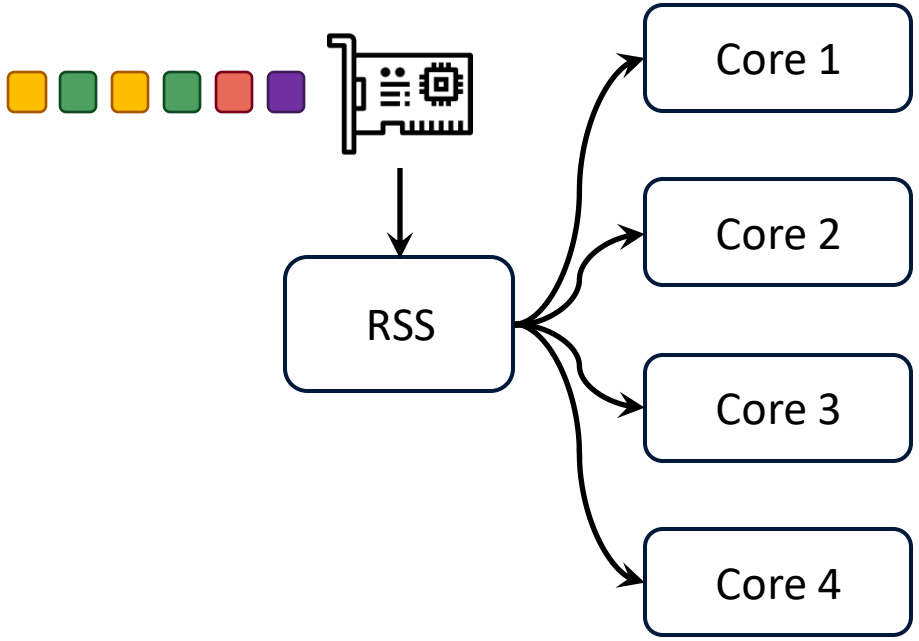
(i) Efficient Inter-Core Load Balancing

⚠ RSS **struggles** to efficiently distribute packets among cores with **adversarial loads**



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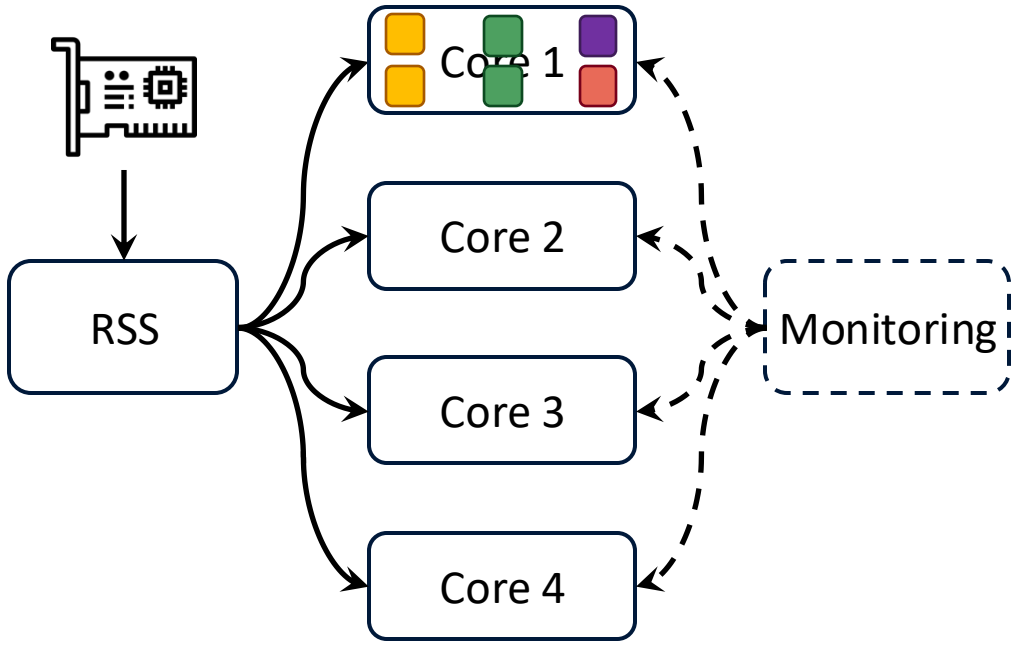

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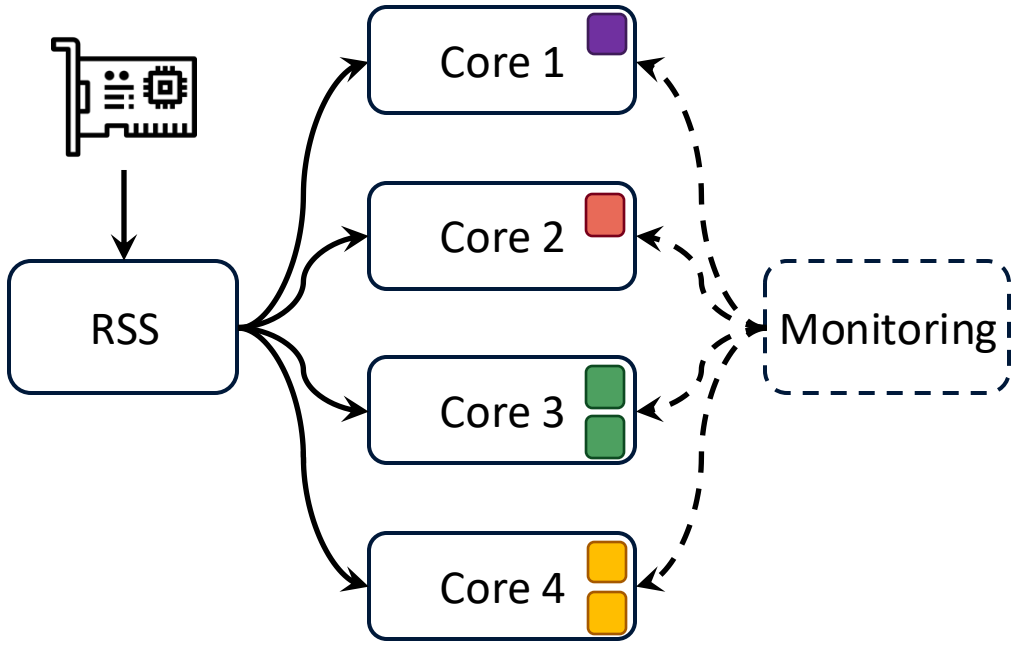

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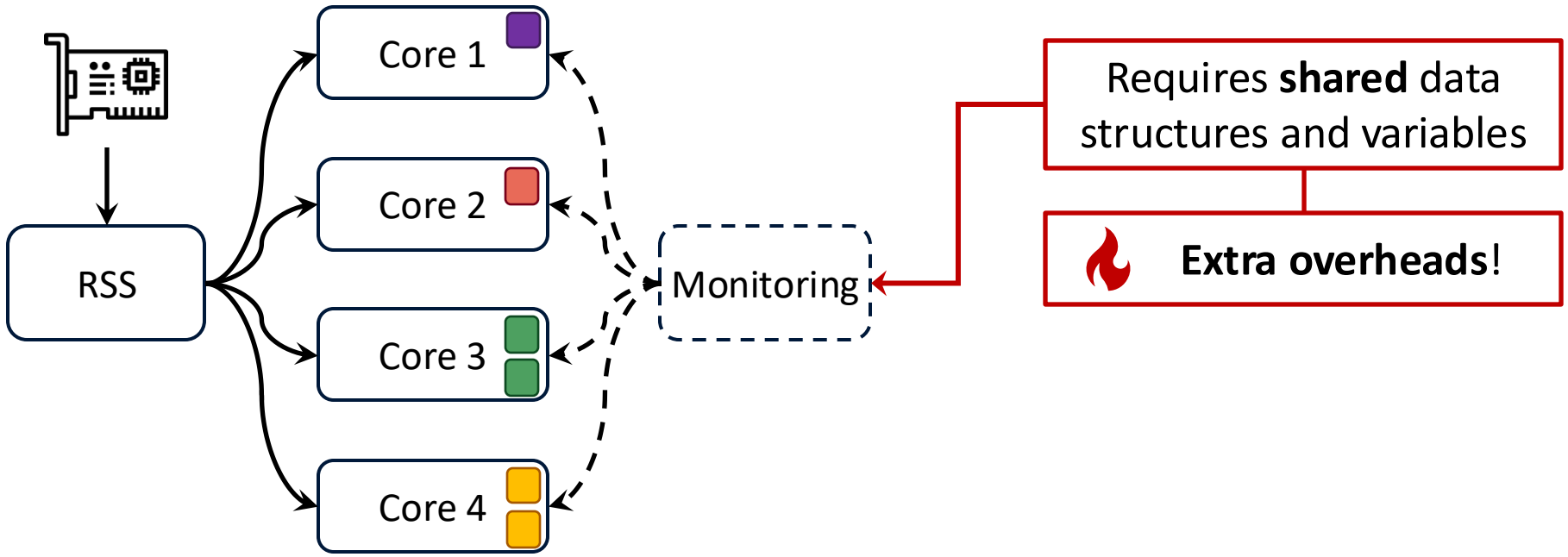

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(i) Efficient Inter-Core Load Balancing

(ii) Stateful NFs with Diverse Flow Definitions

The definition of state is **not exclusively** the 5-tuple!

What happens if they are **chained together**?

Load Balancer	Src IP	Dst IP	Src Port	Dst Port	Protocol
Policer	Src IP	Dst IP	Src Port	Dst Port	Protocol
Port Scan Detector	Src IP	Dst IP	Src Port	Dst Port	Protocol

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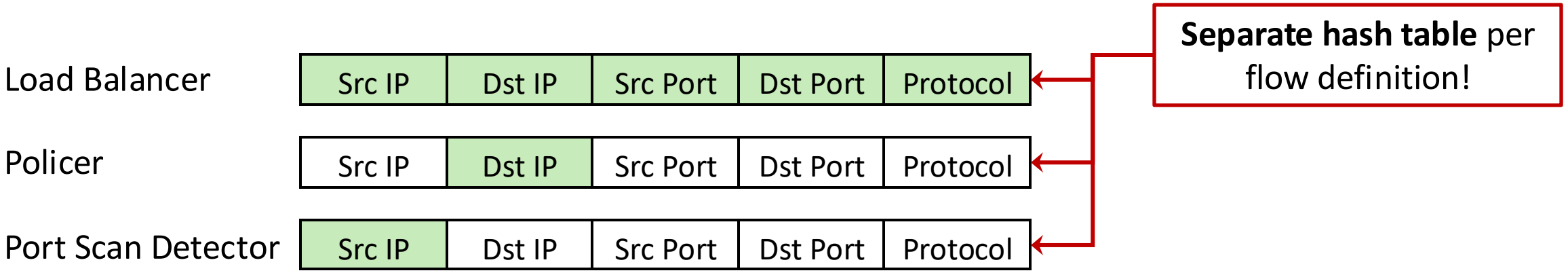

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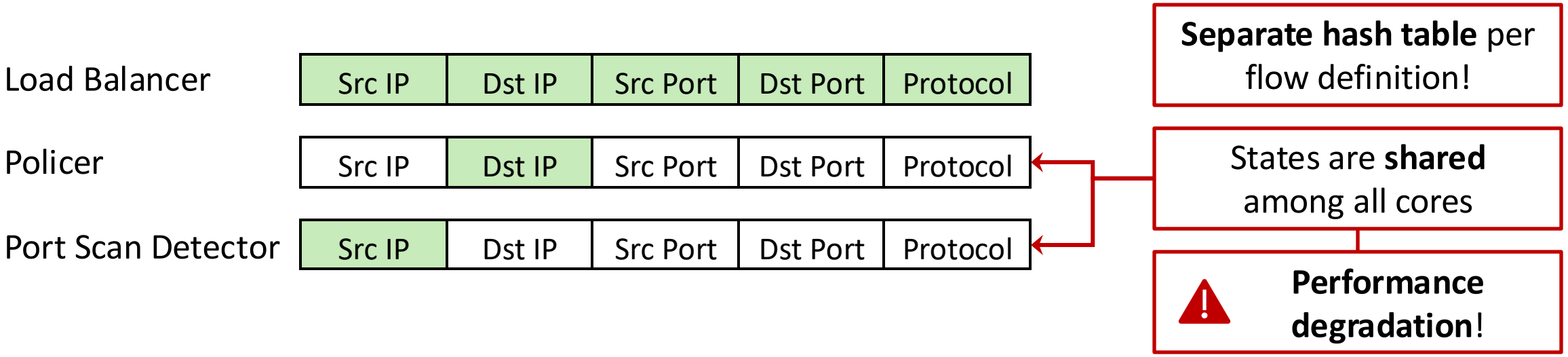

Essential Principles of Stateful Packet Processors

✓ **VPP**
Batch Processing

✓ **FastClick**
Minimize Memory Accesses

?
Minimize Sync. Overheads

Overlooking one of these principles **hinders**
Stateful NF frameworks to process >100Mpps

We **must** support the three principles **together**!

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Batch Processing **Minimize Memory Accesses** **Minimize Sync. Overheads**

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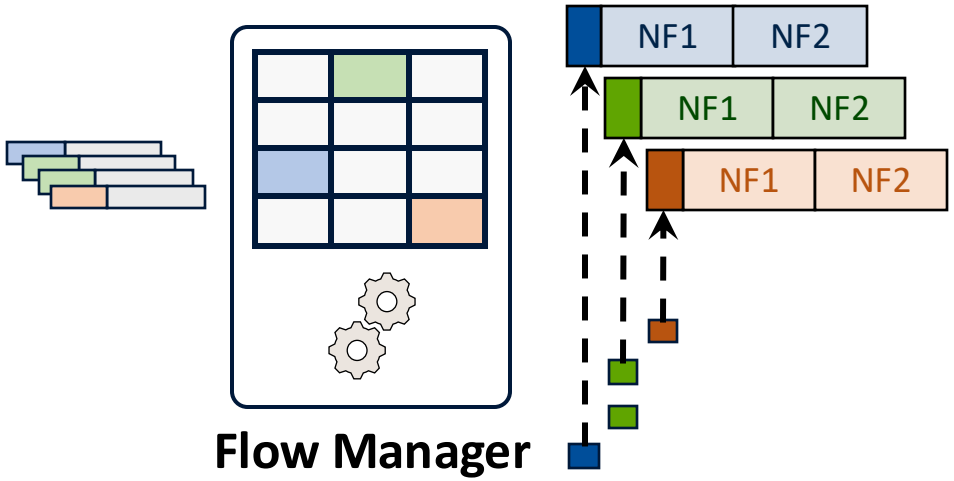
Batch Processing **Minimize Memory Accesses** **Minimize Sync. Overheads**

- **Optimized** state aggregation
- **Bulk Lookup** for **all packets** in the batch



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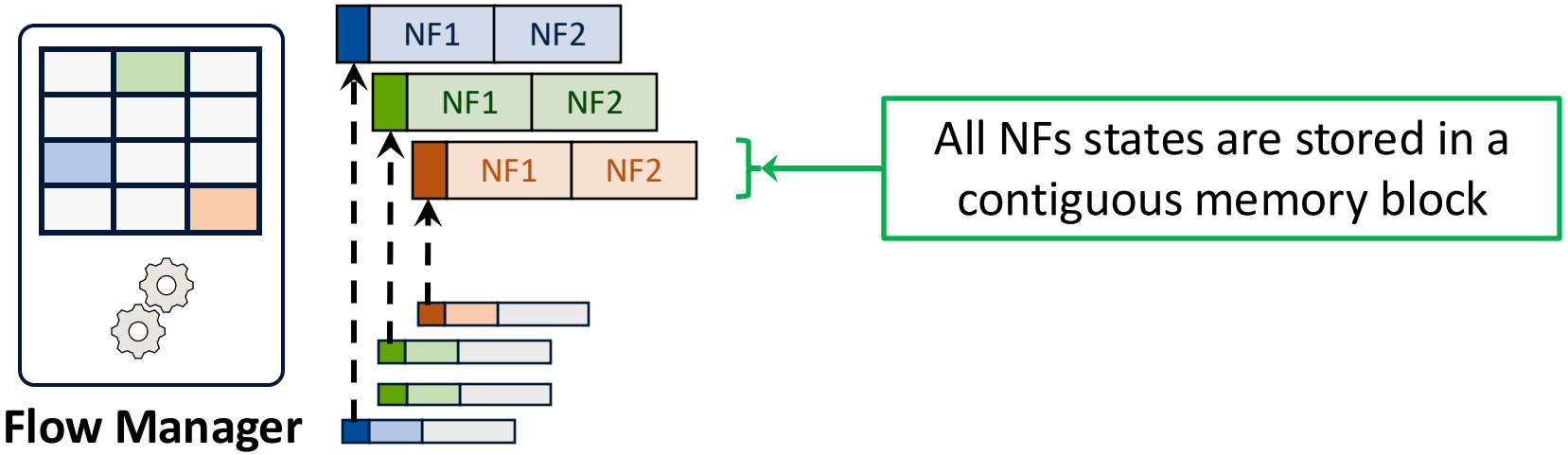
Batch Processing **Minimize Memory Accesses** **Minimize Sync. Overheads**

- **Optimized** state aggregation
- **Bulk Lookup** for **all packets** in the batch → **Batches are preserved!**



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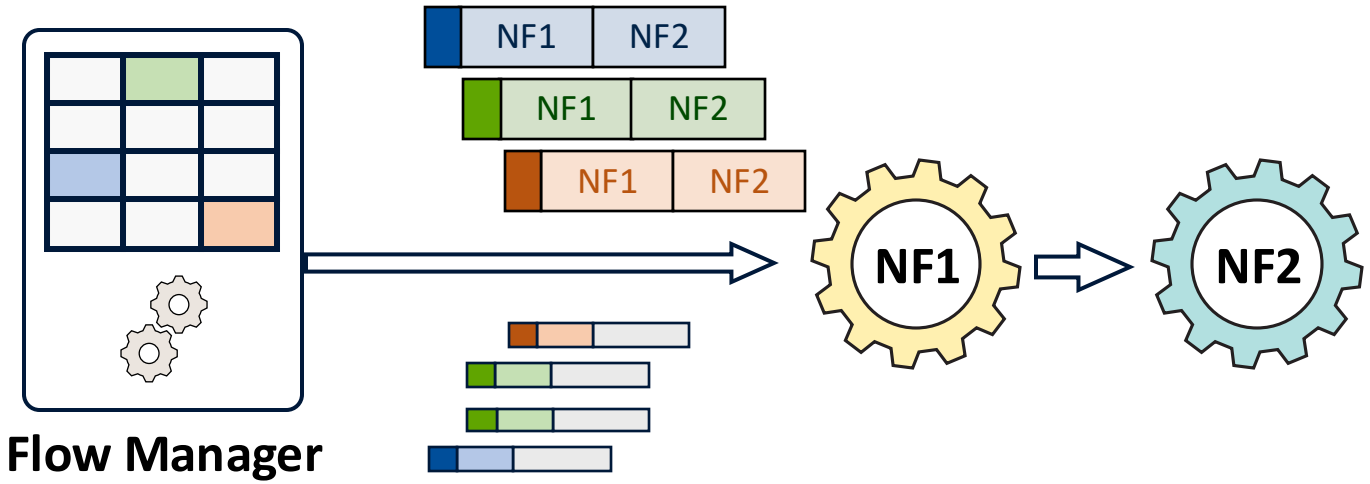

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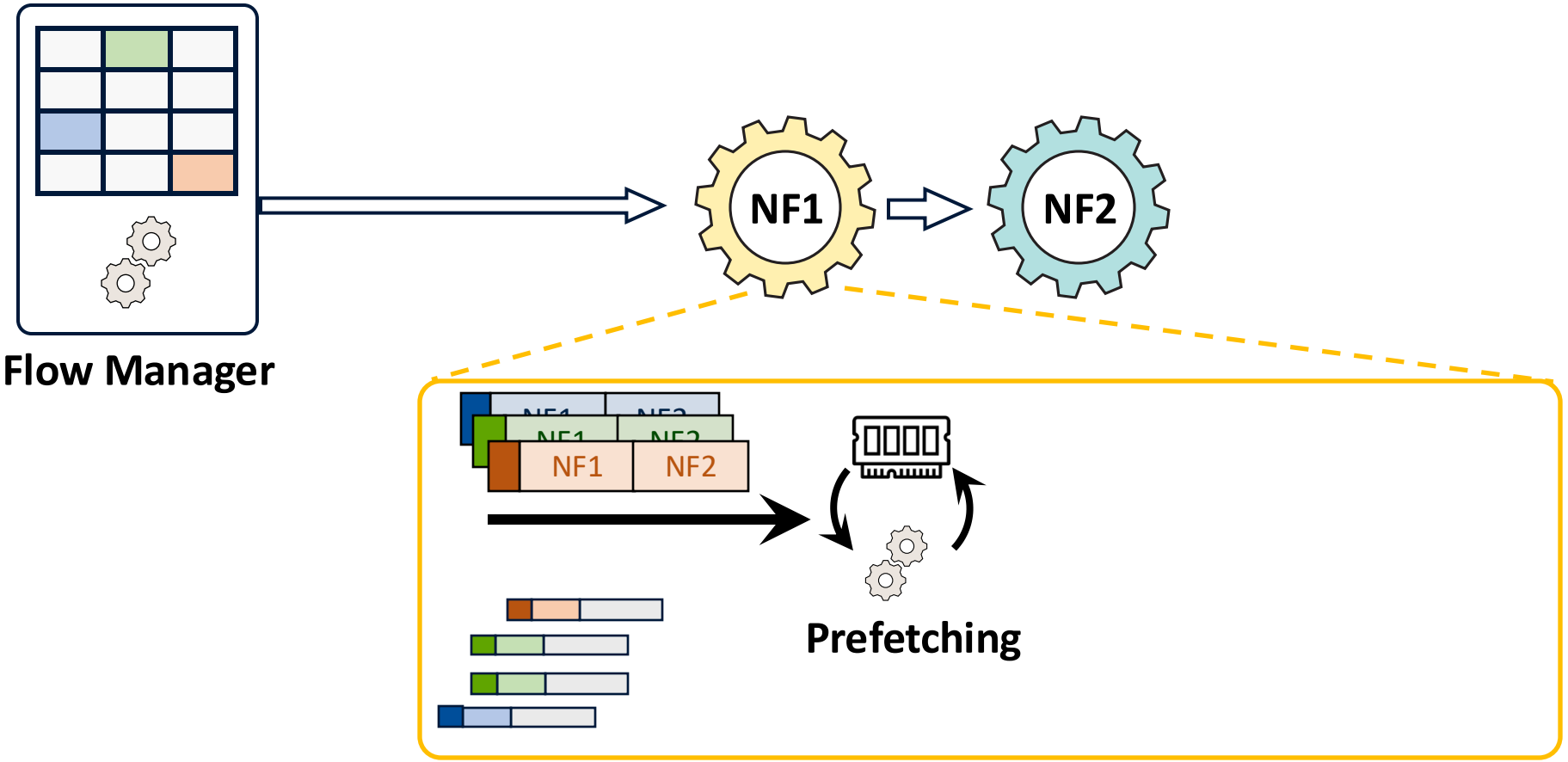
Batch Processing **Minimize Memory Accesses** **Minimize Sync. Overheads**

✓ Each NF **prefetches** its state data at the **right time**



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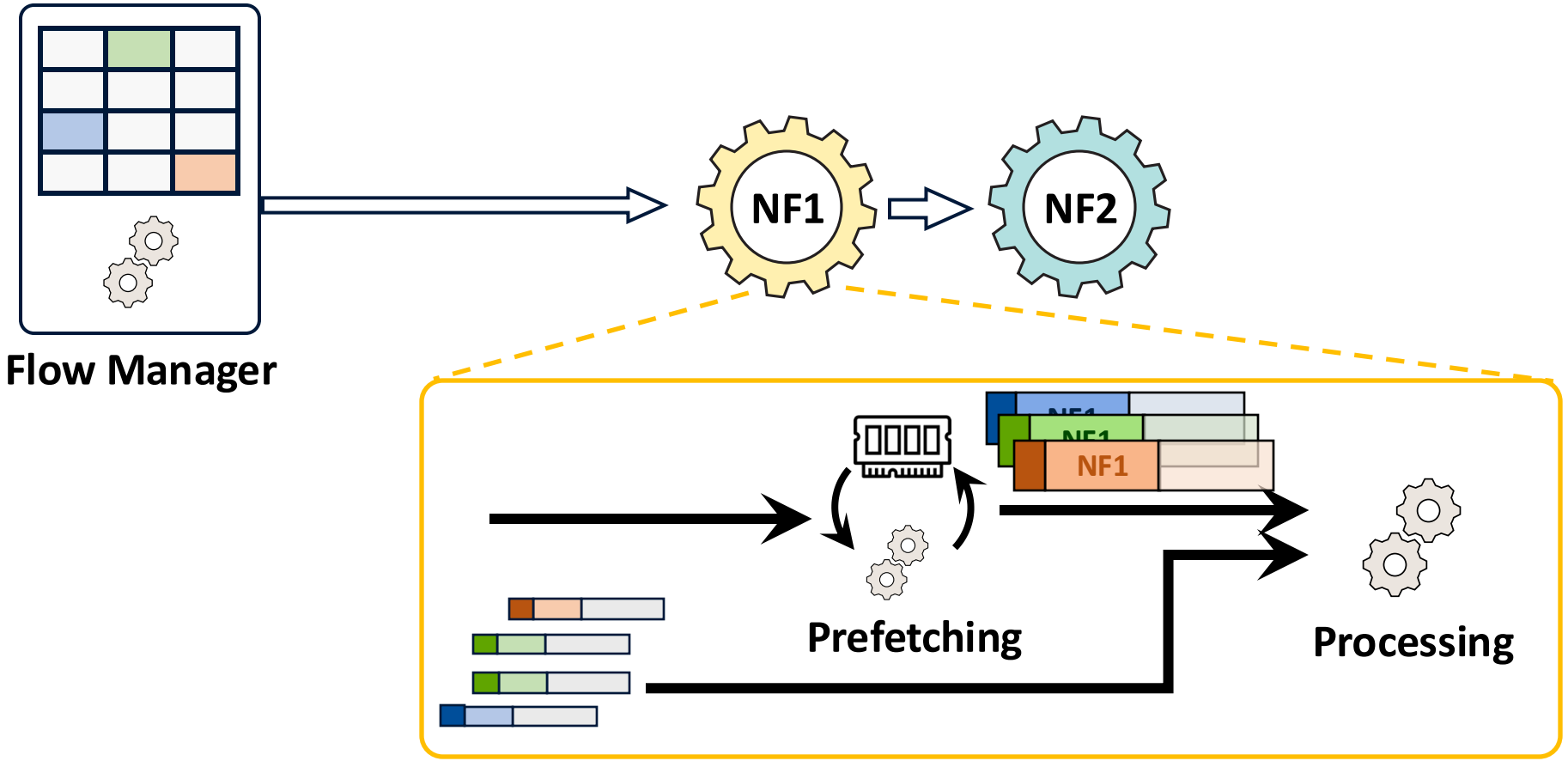
Batch Processing **Minimize Memory Accesses** **Minimize Sync. Overheads**

✓ Each NF **prefetches** its state data at the **right time** ➡ **Minimize memory loads overheads**



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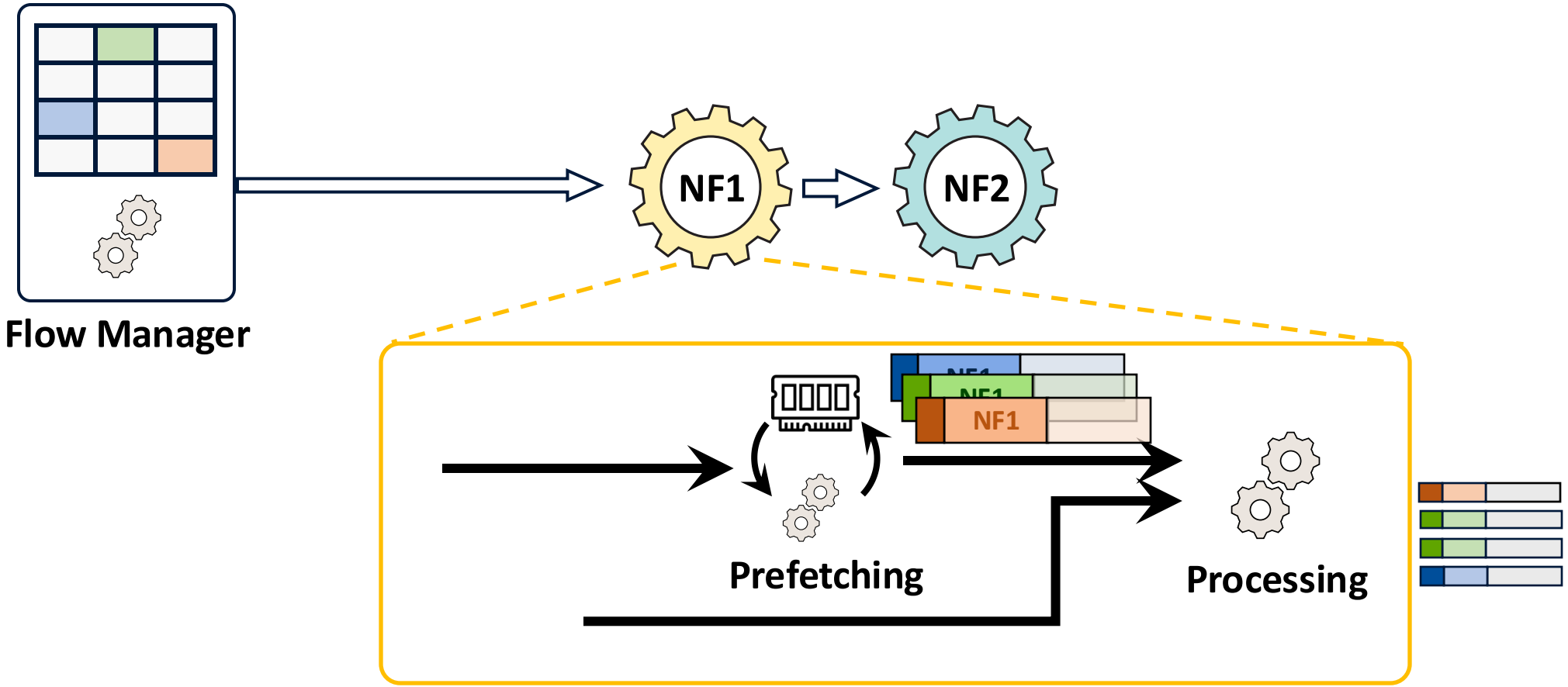
Batch Processing **Minimize Memory Accesses** **Minimize Sync. Overheads**

⚠ Only considers 5-tuple flows definition!



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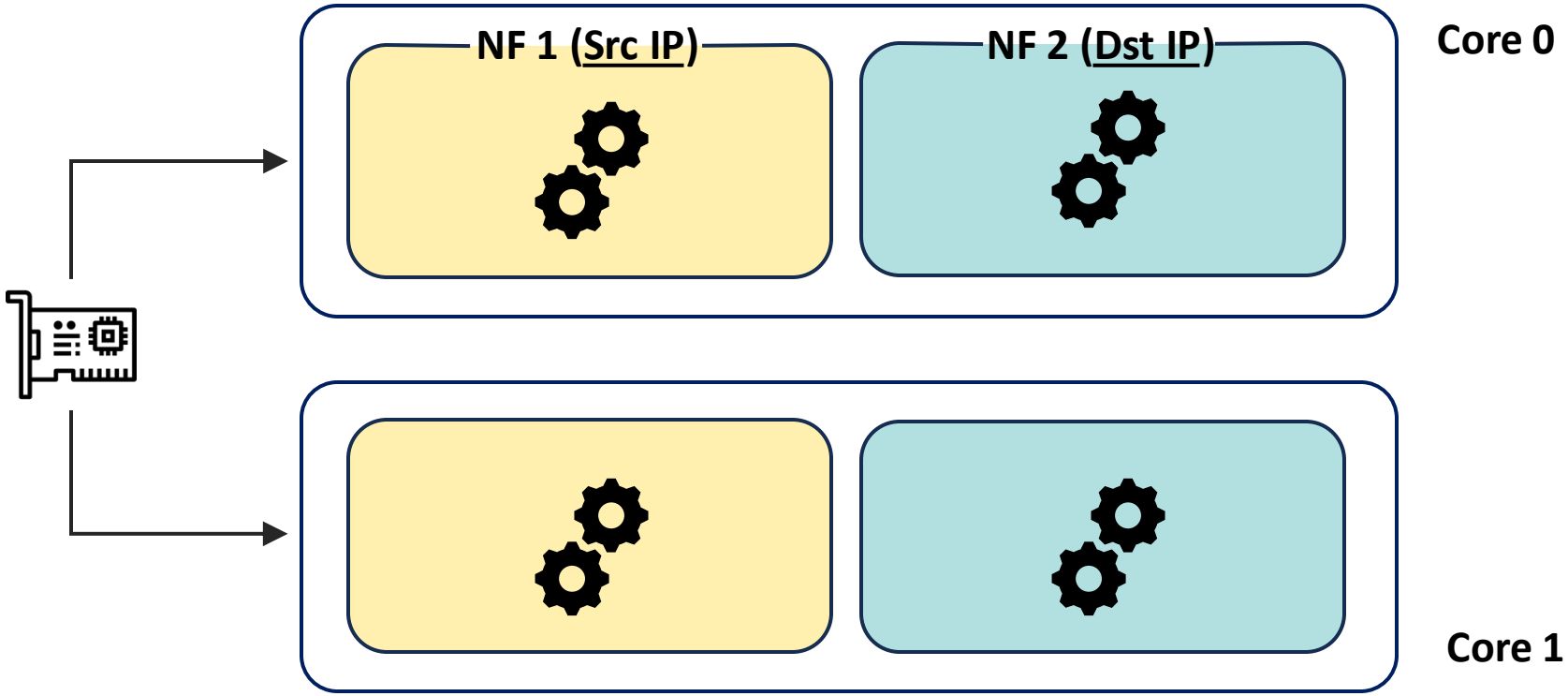

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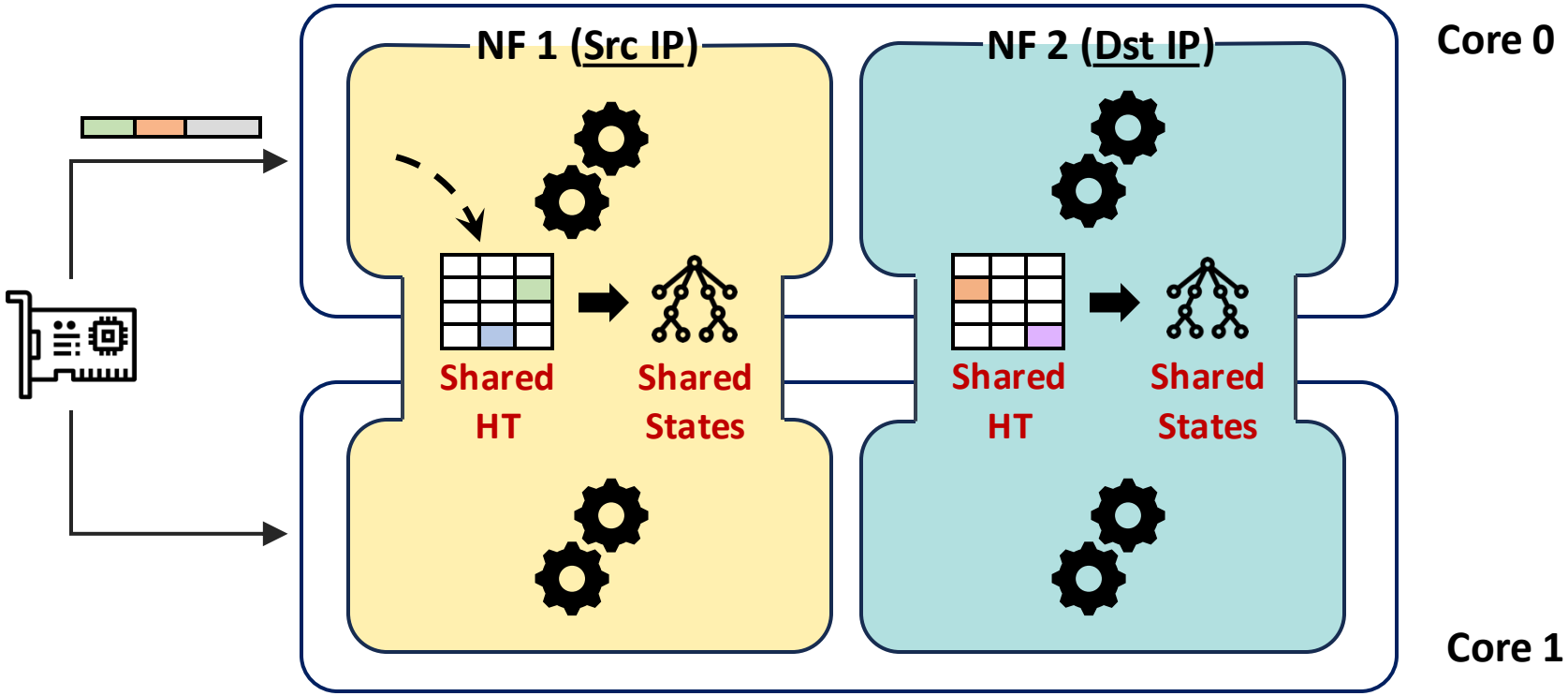

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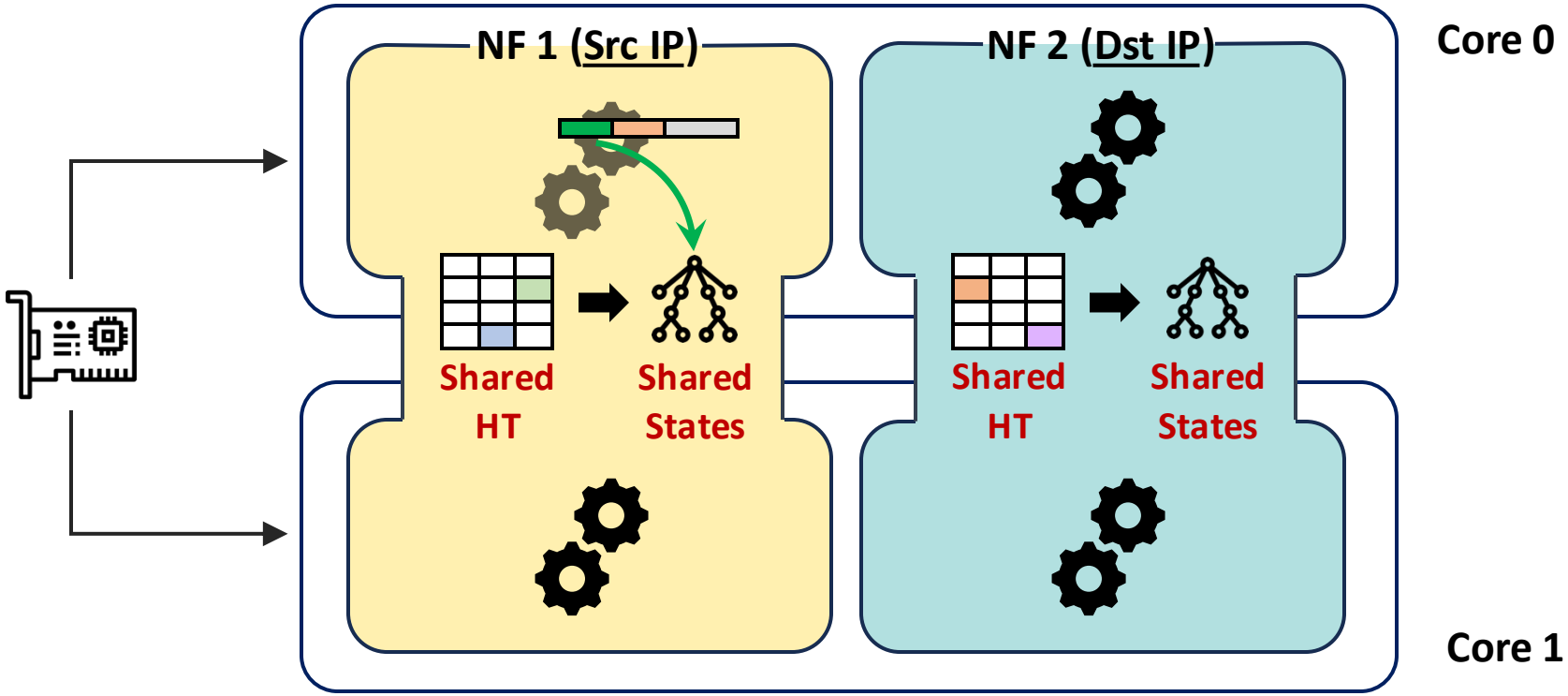

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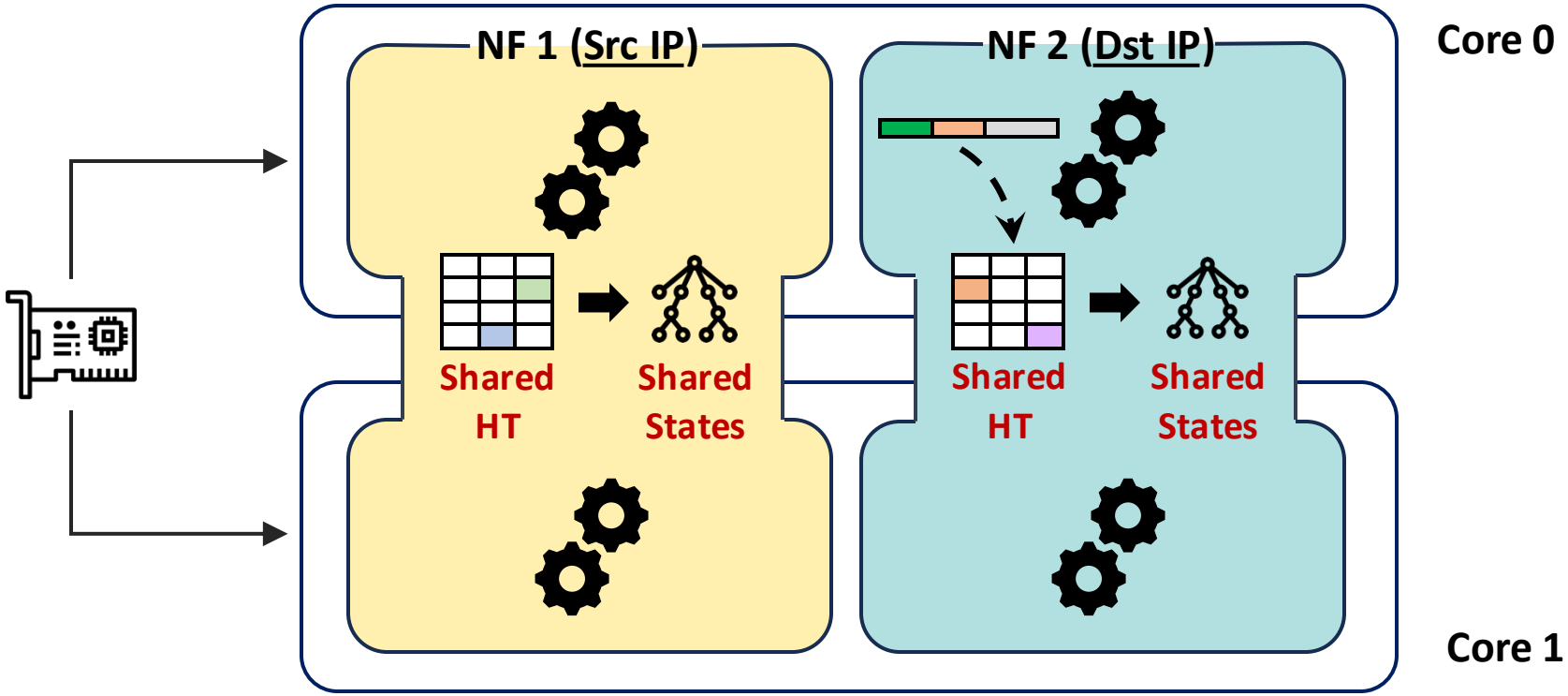

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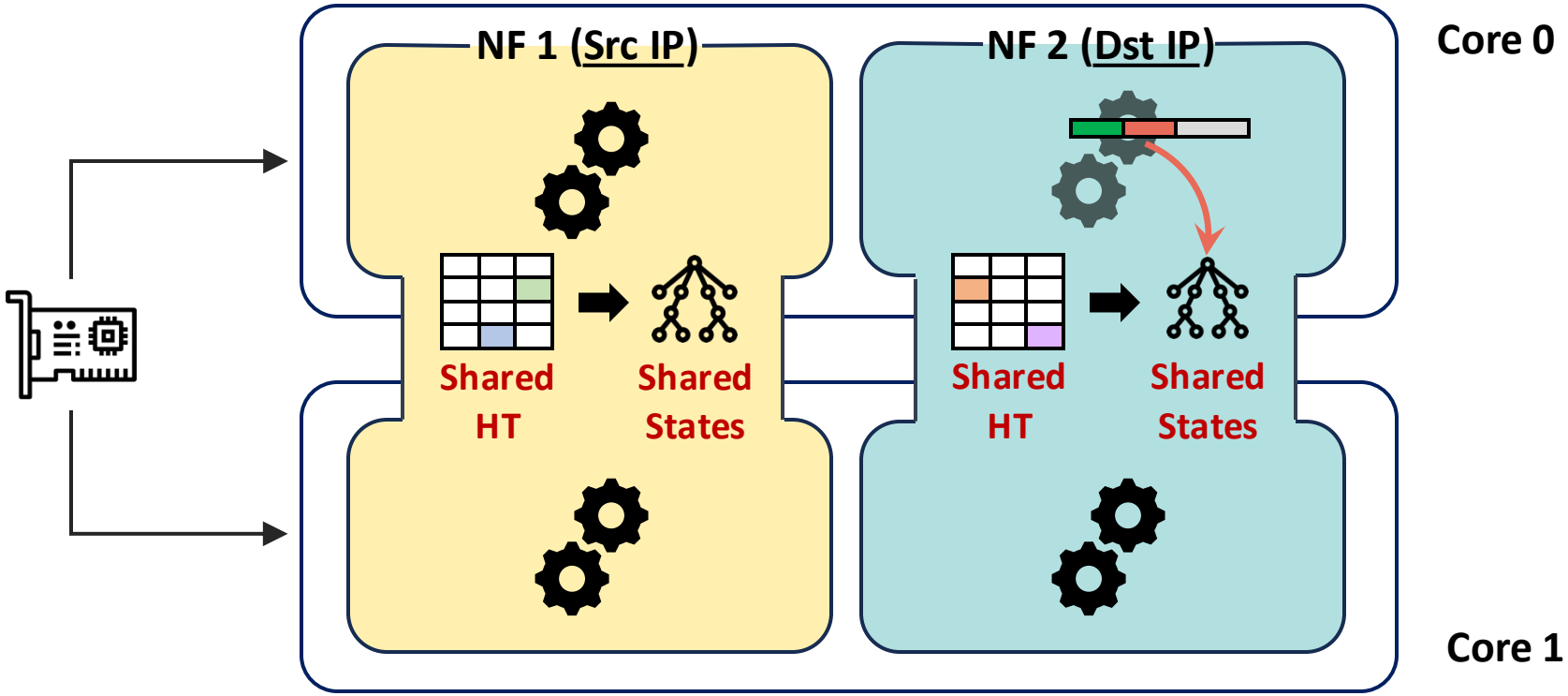

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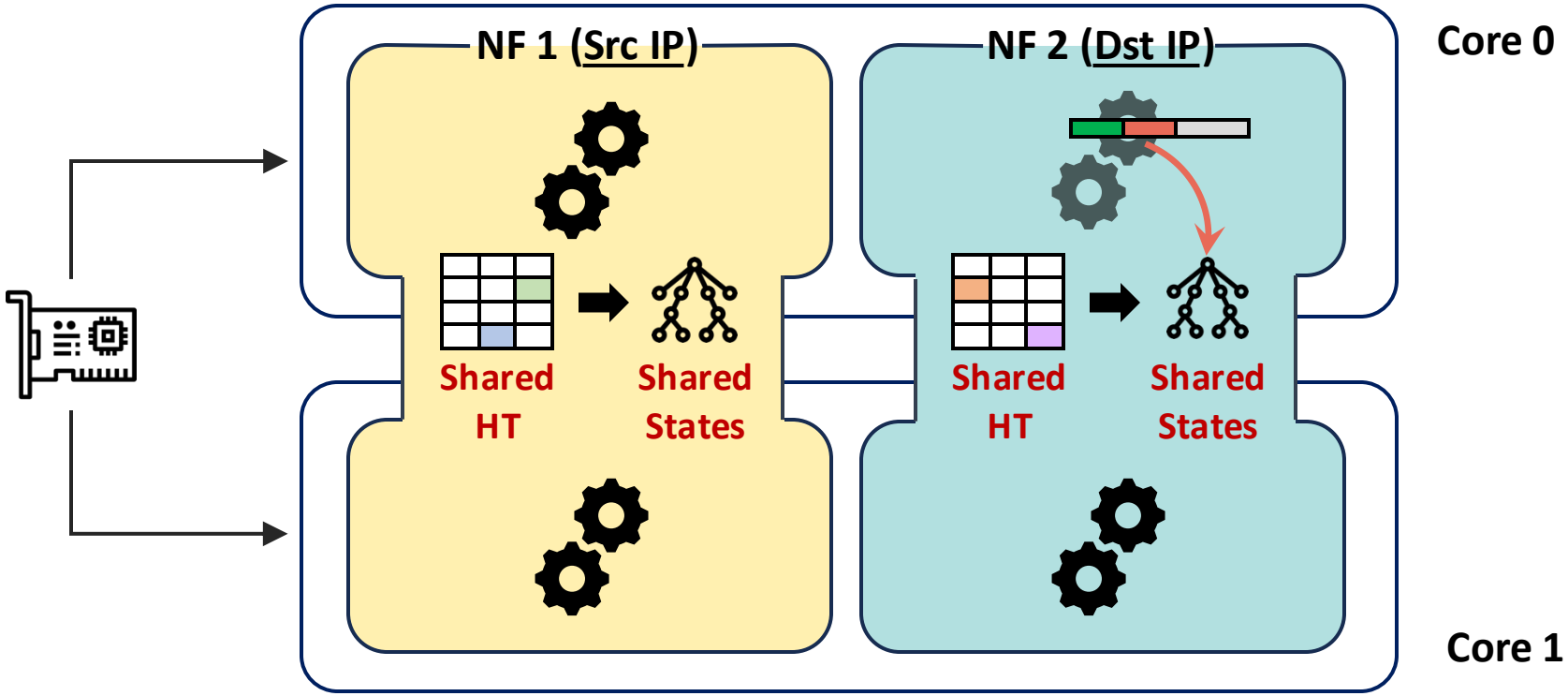
How can we **reduce** the **inevitable** sync. overhead with different flow definitions?



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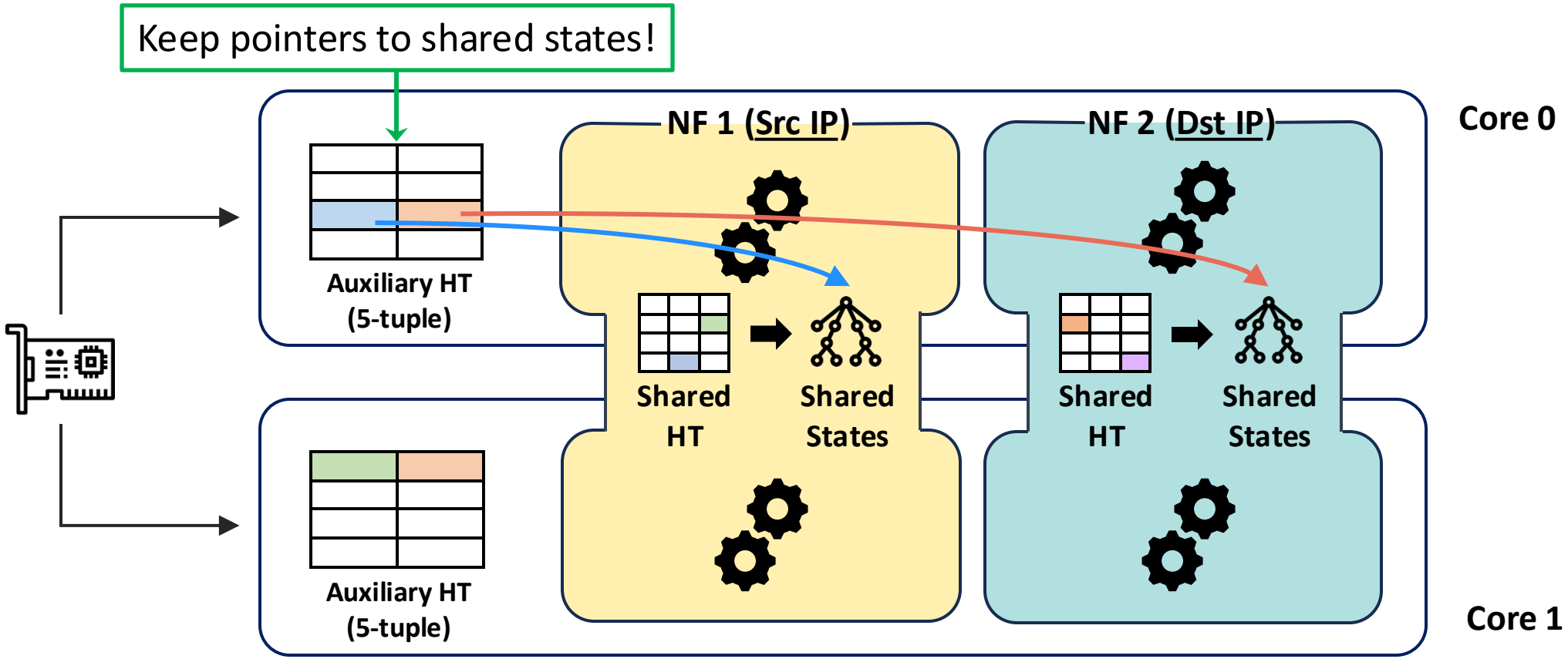

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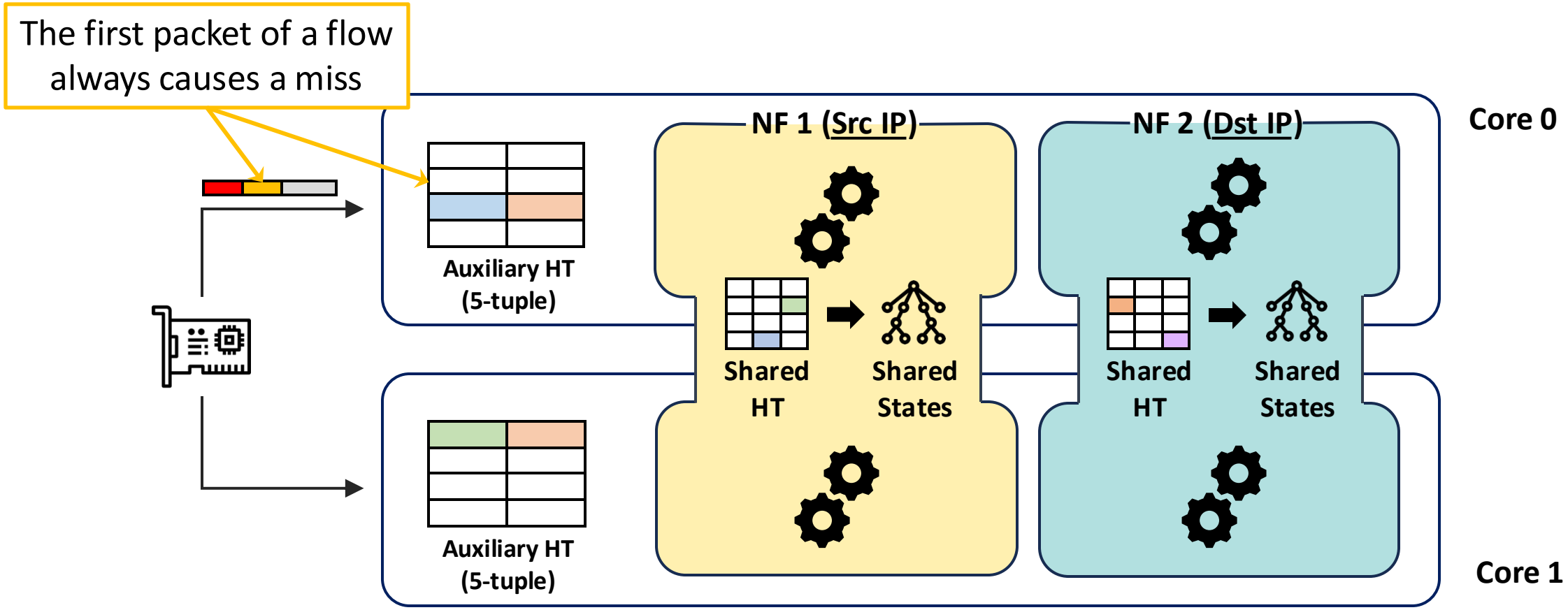

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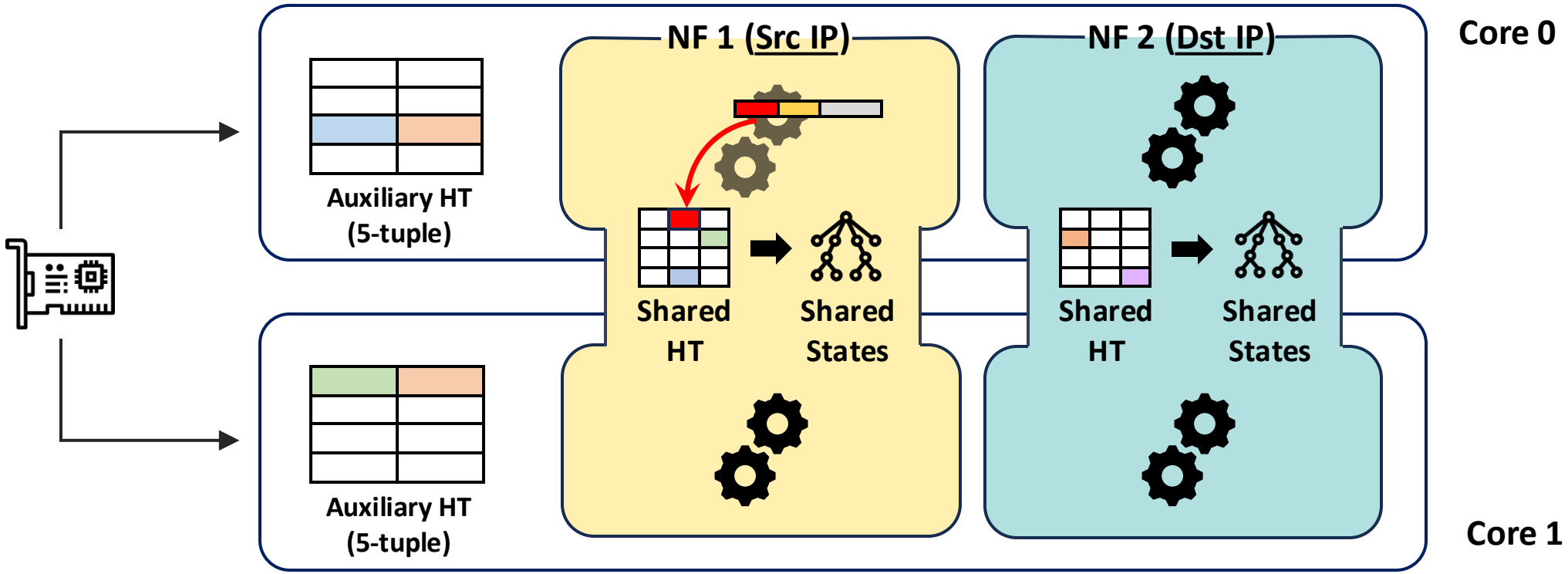

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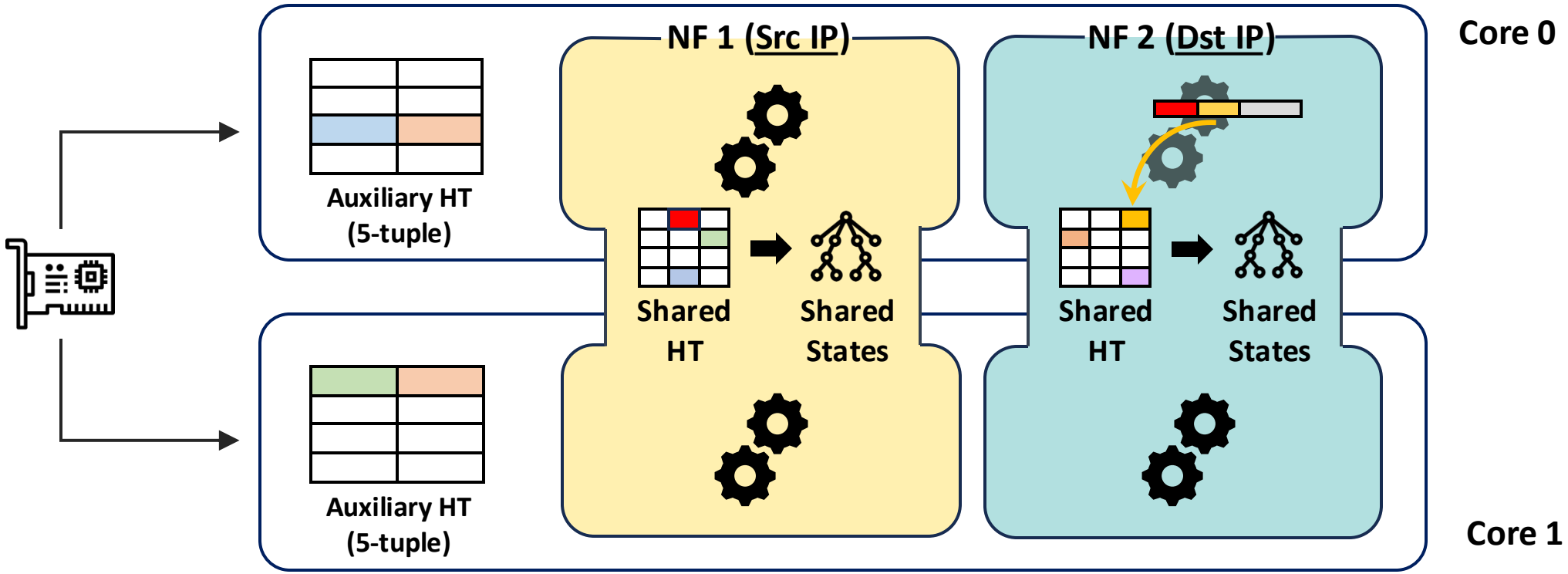

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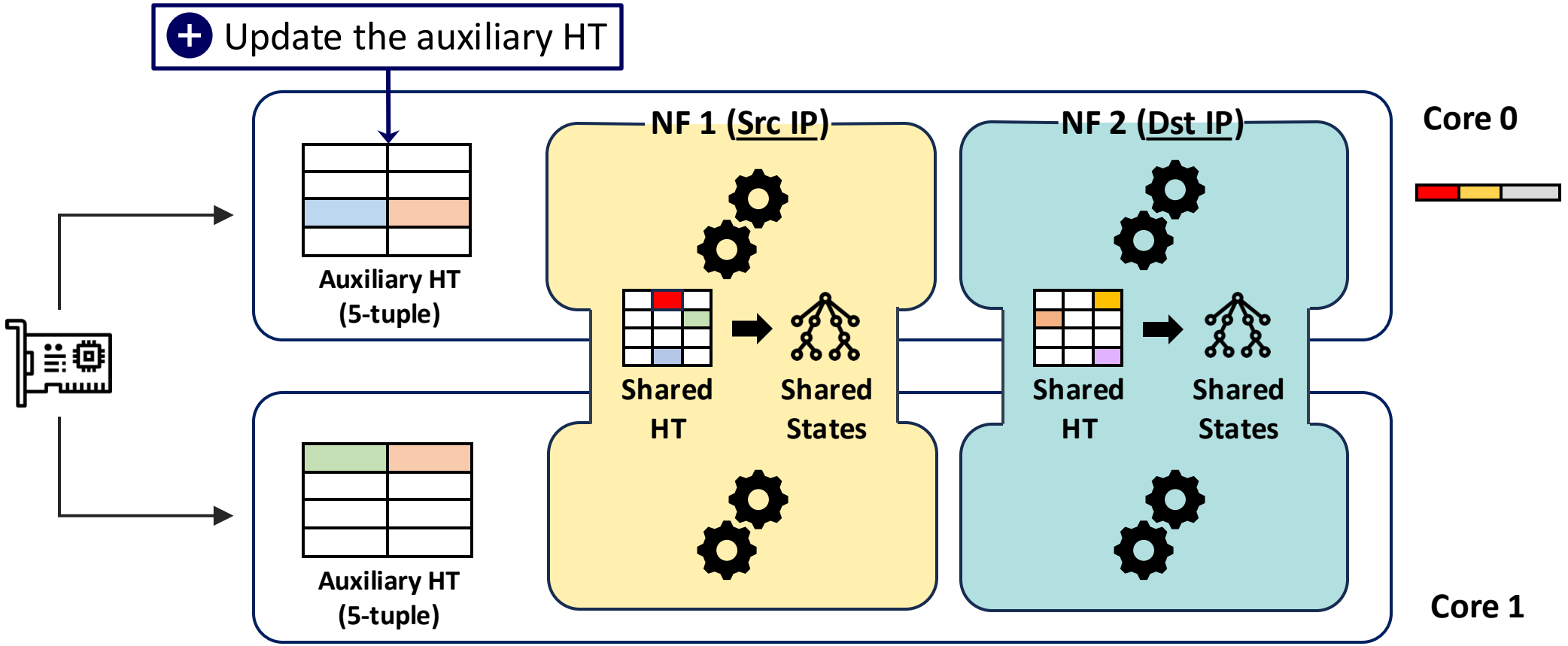
How can we **reduce** the **inevitable** sync. overhead with different flow definitions?



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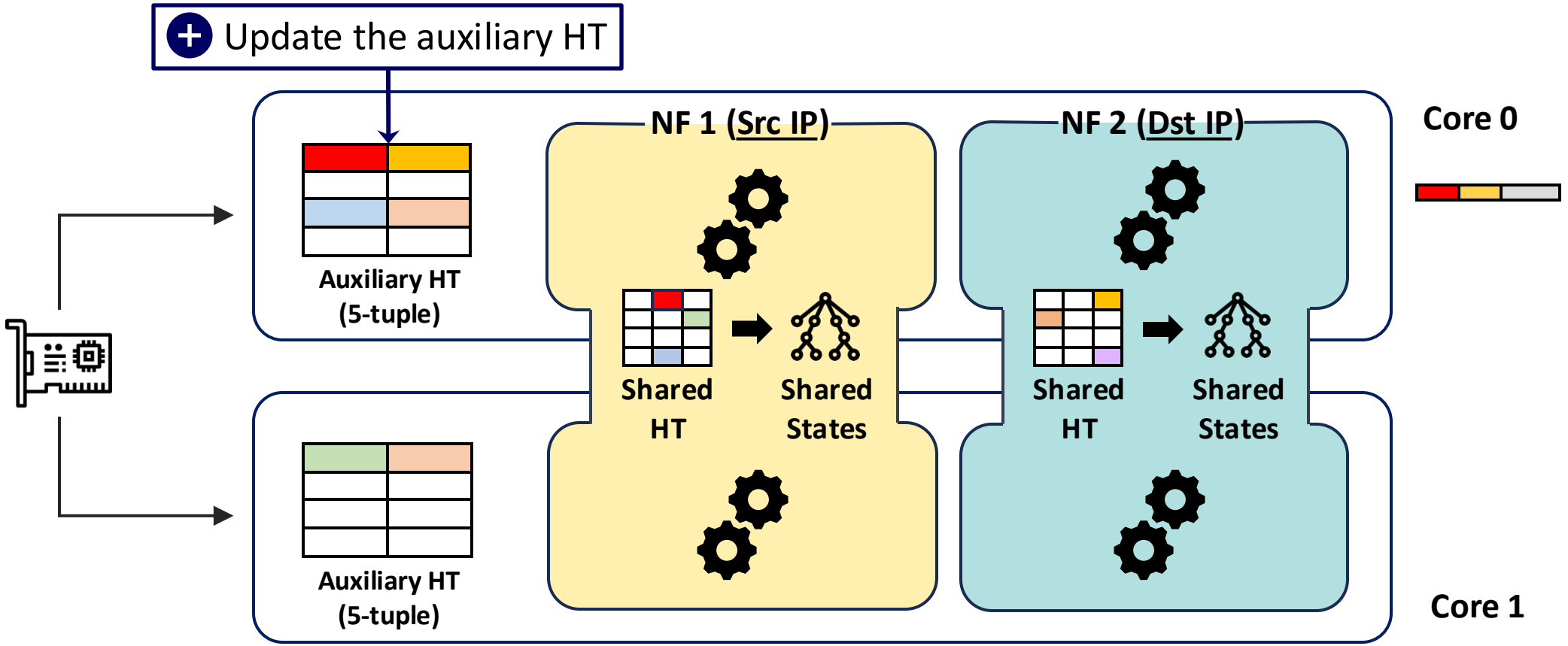

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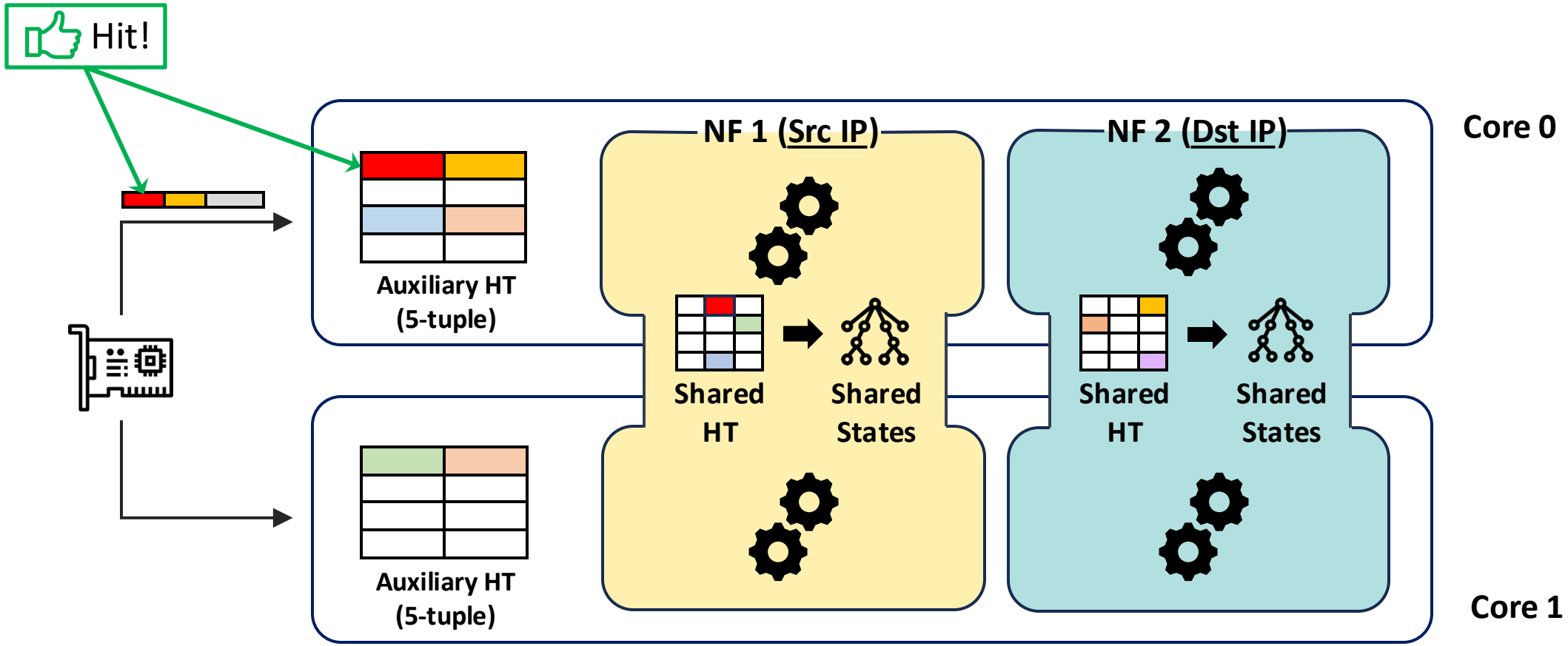

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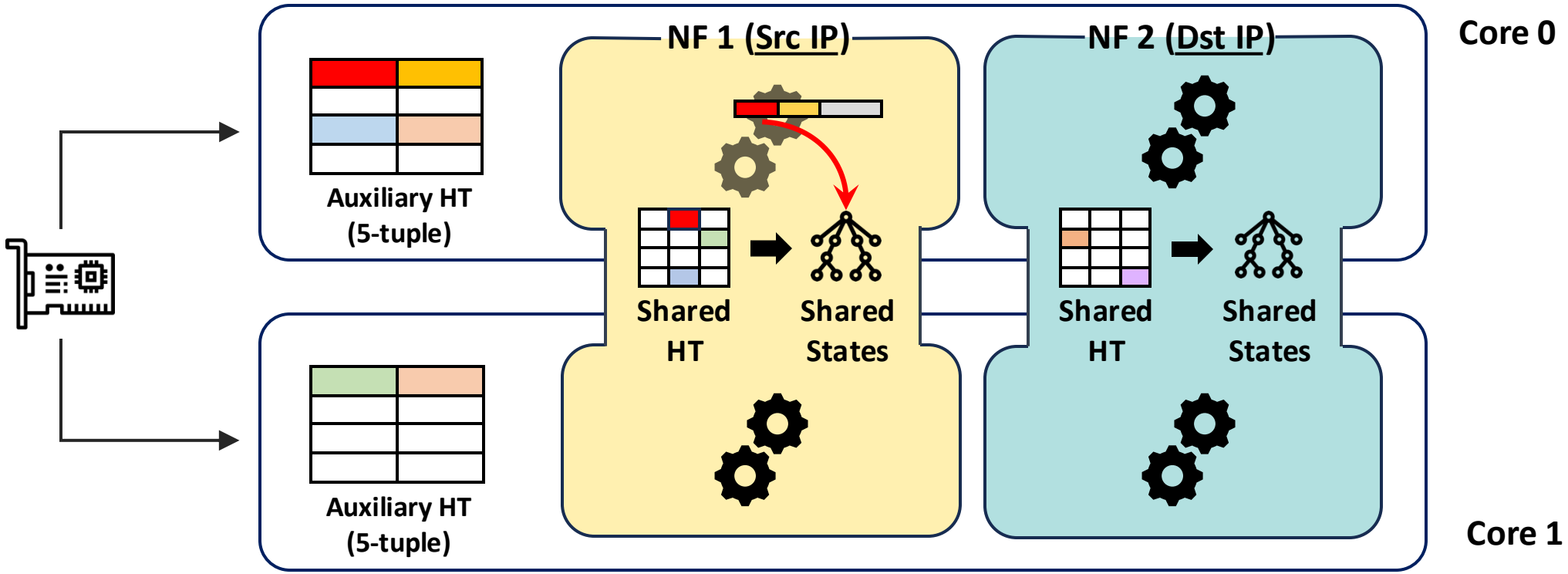

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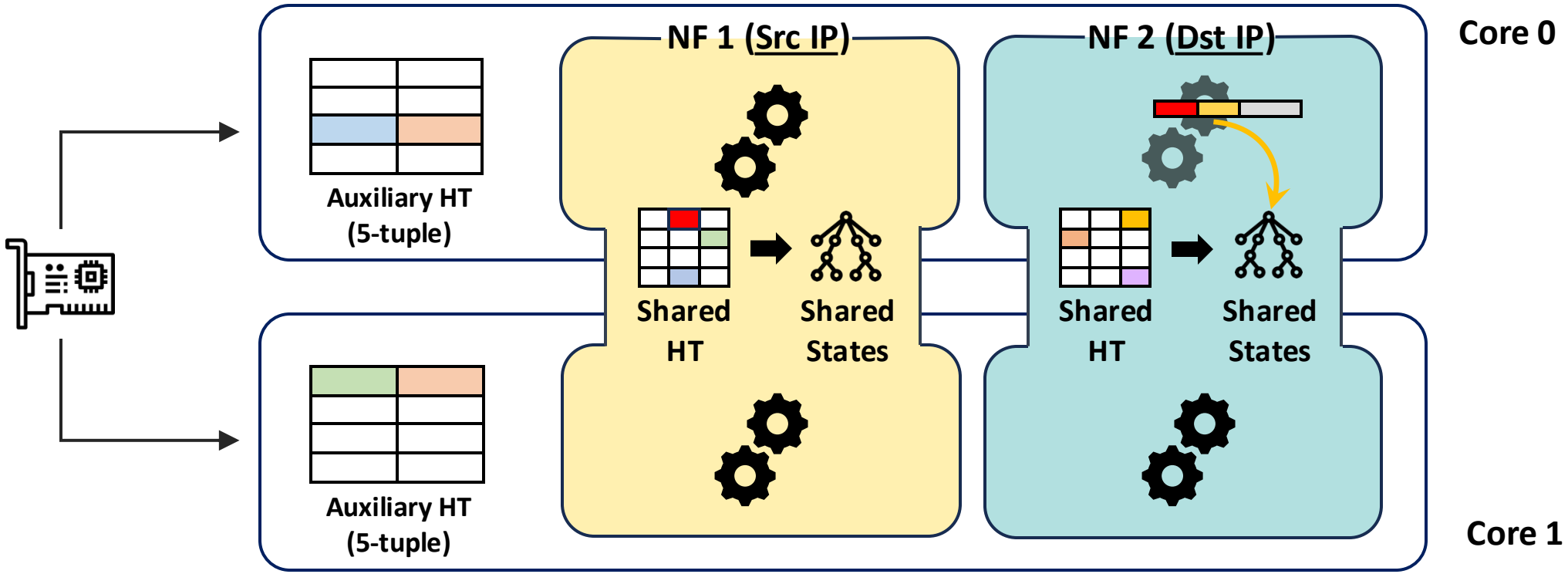

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Batch Processing **Minimize Memory Accesses** **Minimize Sync. Overheads**

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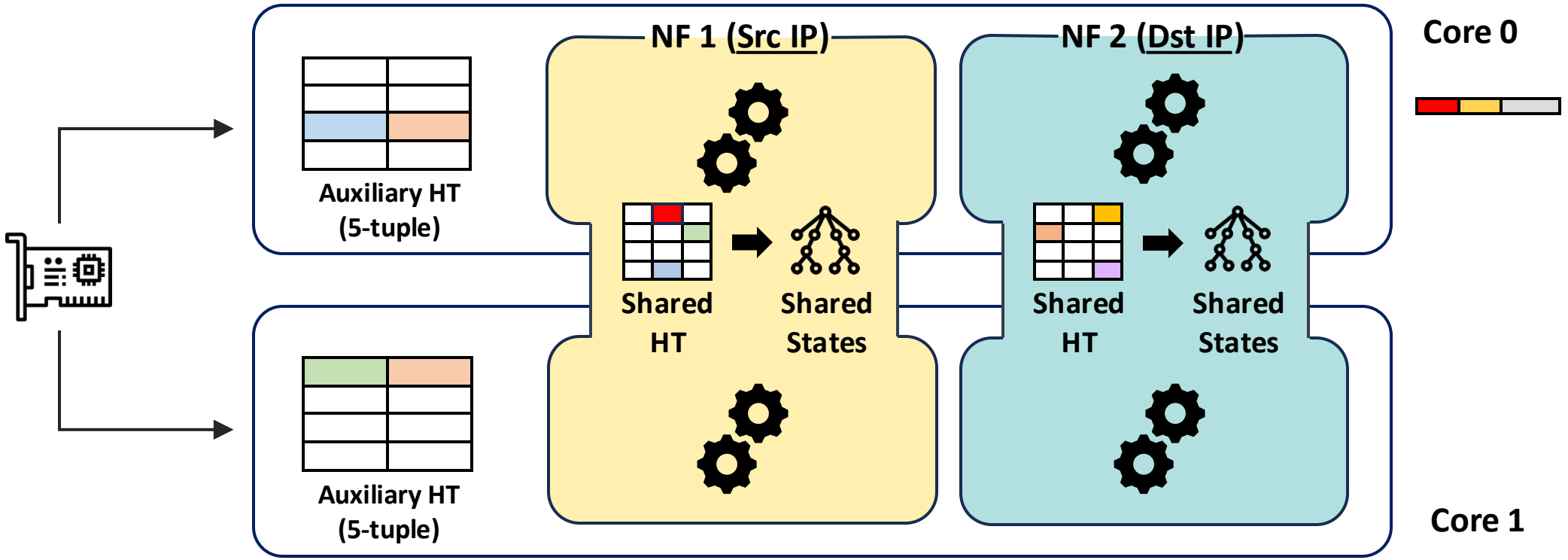
Only a **single expensive** insert/lookup into/from shared HT → **Minimize sync. overheads**



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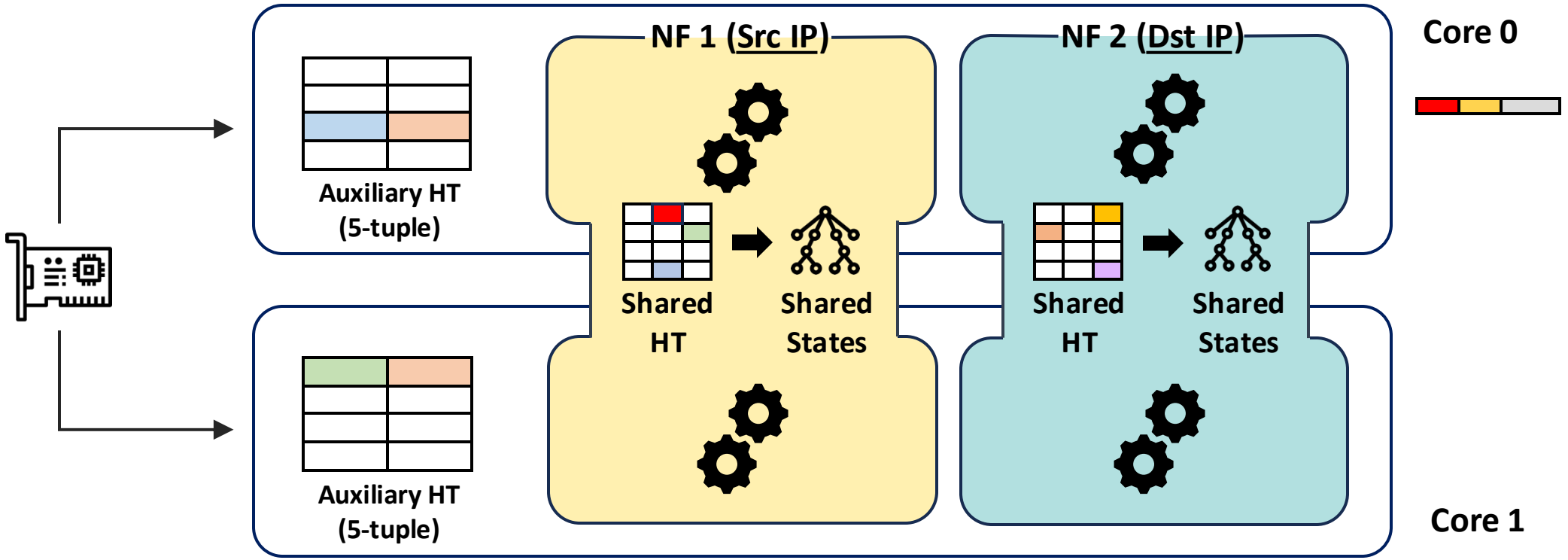
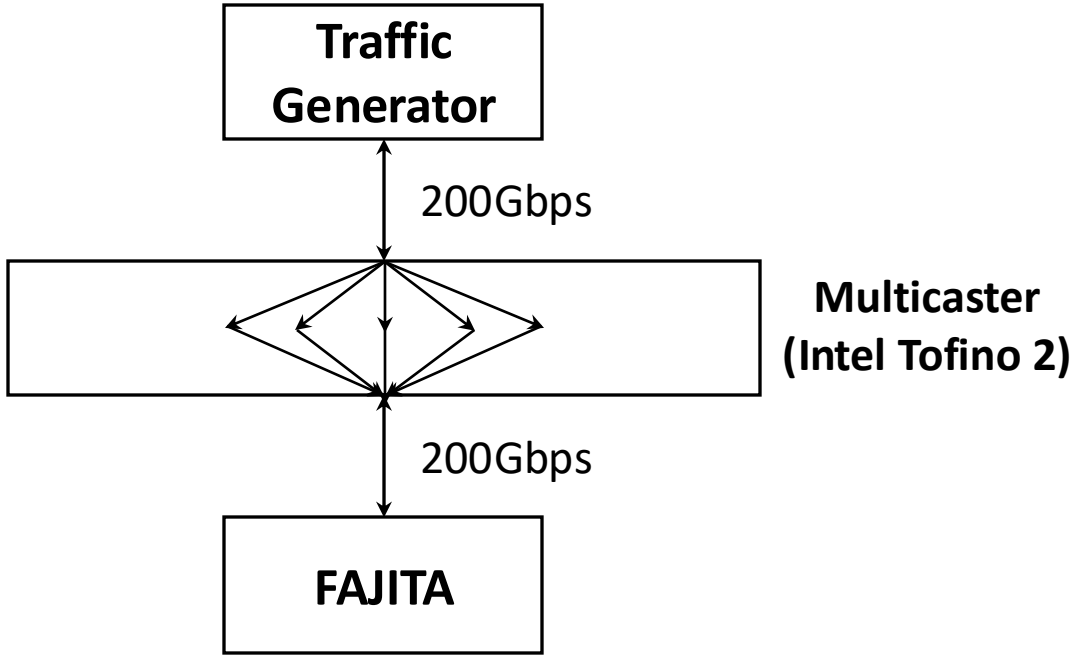


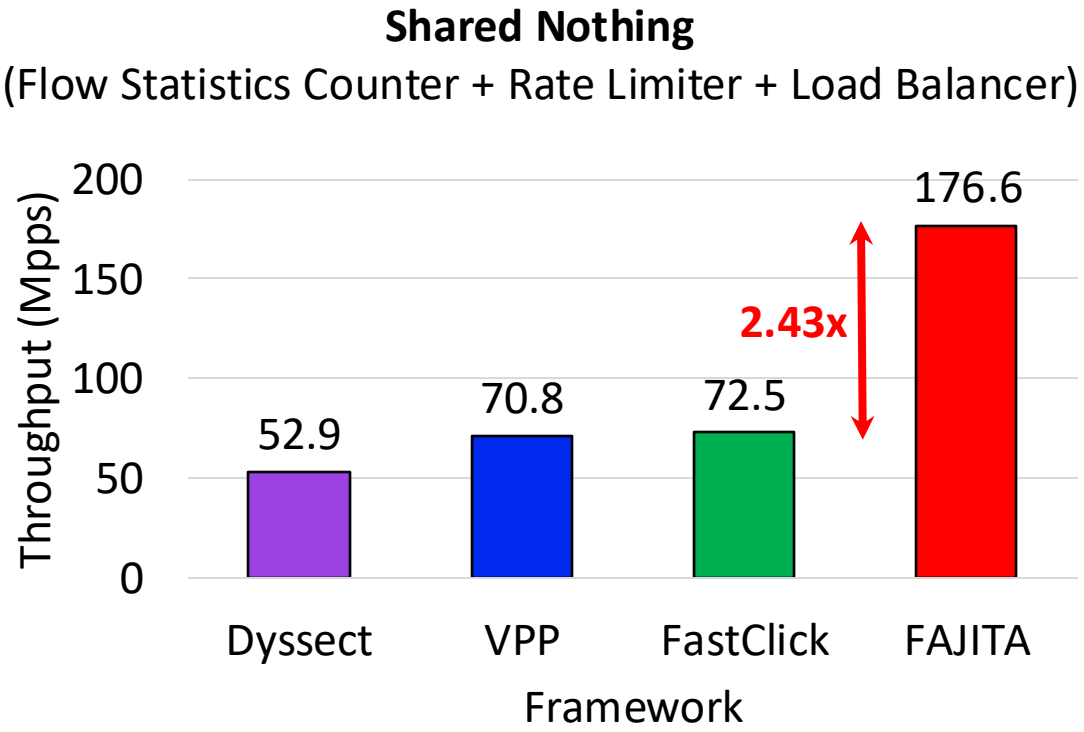
Evaluation

Testbed and Workloads



Evaluation

Does FAJITA Improve Performance?



16 CPU cores

Synthetic 64-B trace w/ 2 million flows

Evaluation

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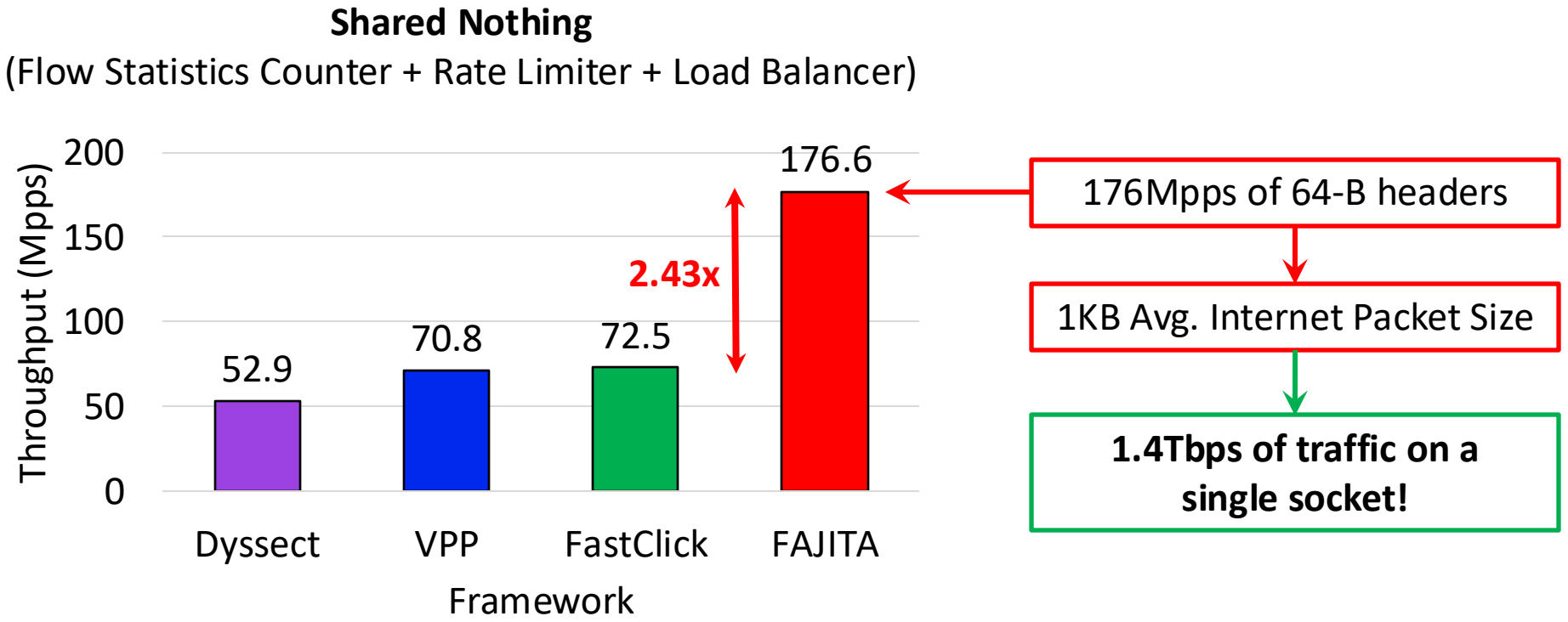

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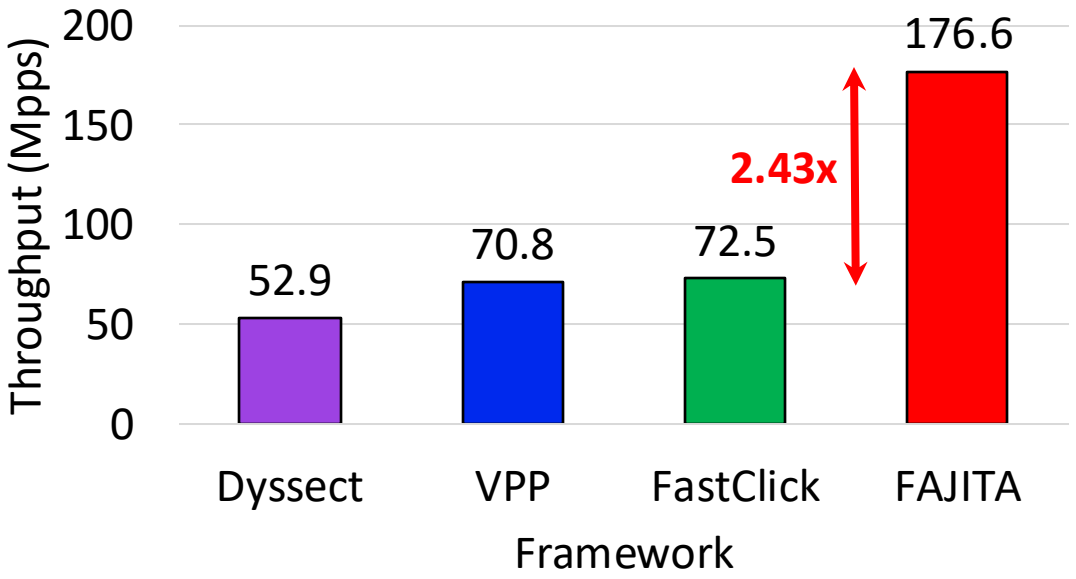
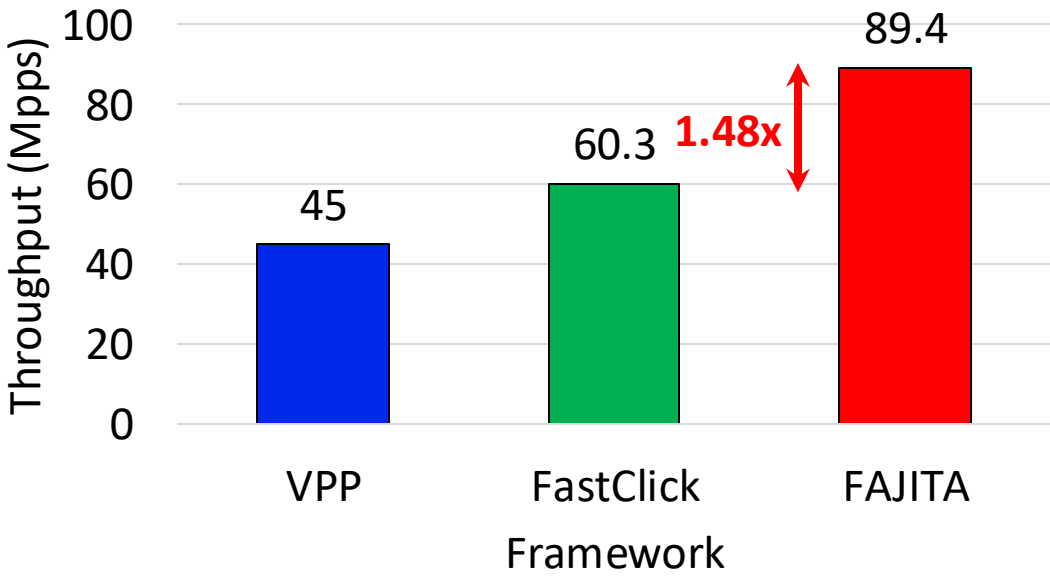
Shared Nothing
(Flow Statistics Counter + Rate Limiter + Load Balancer)



Shared
(Src IP Counter + Policer + Load Balancer)



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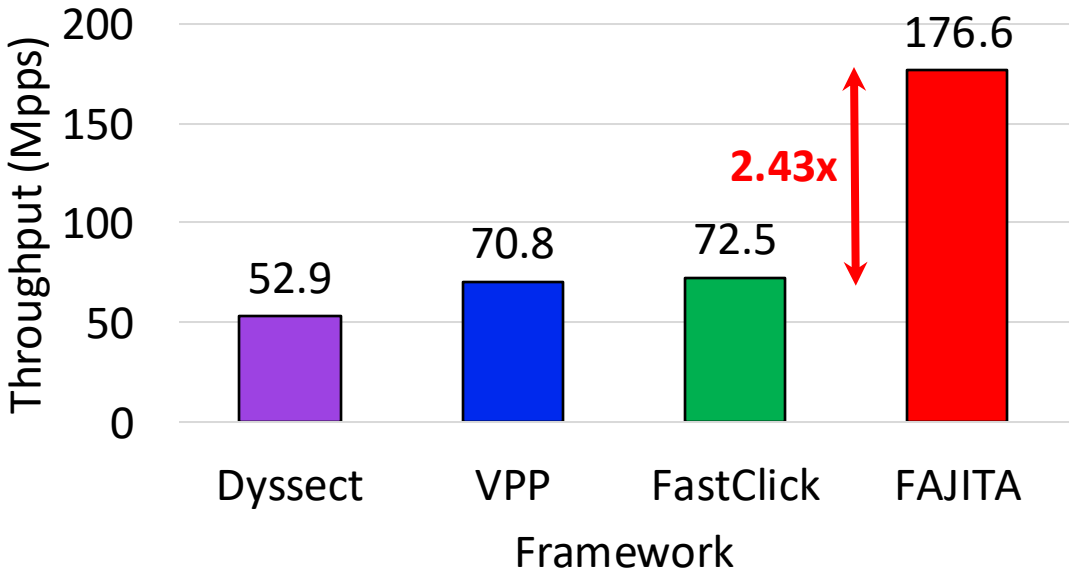
Evaluation

Does FAJITA Improve Performance?

FAJITA is the first system to enable **>100Mpps stateful NF chains** on a **single socket**!

Shared Nothing
(Flow Statistics Counter + Rate Limiter + Load Balancer)



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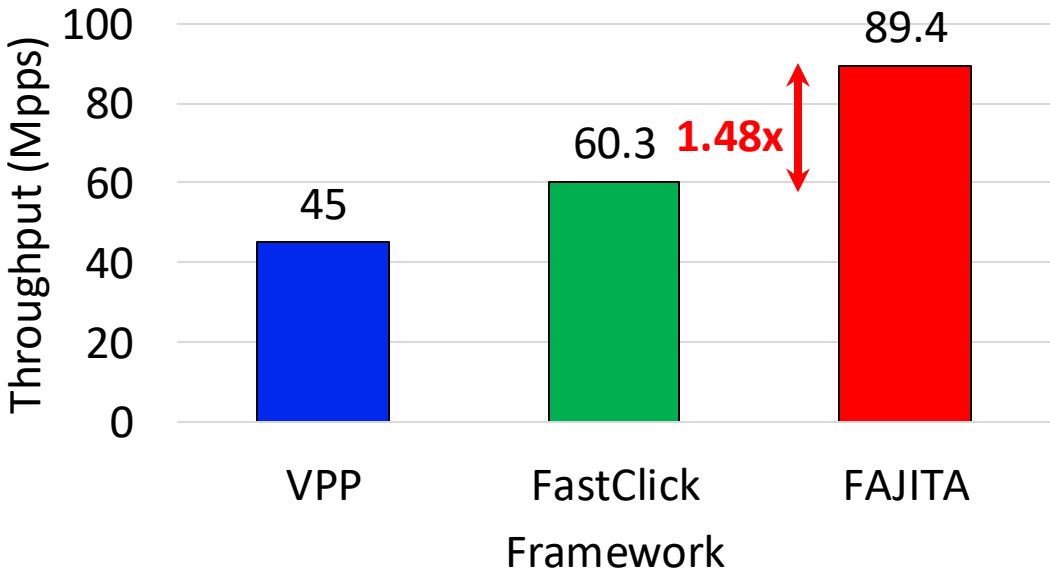
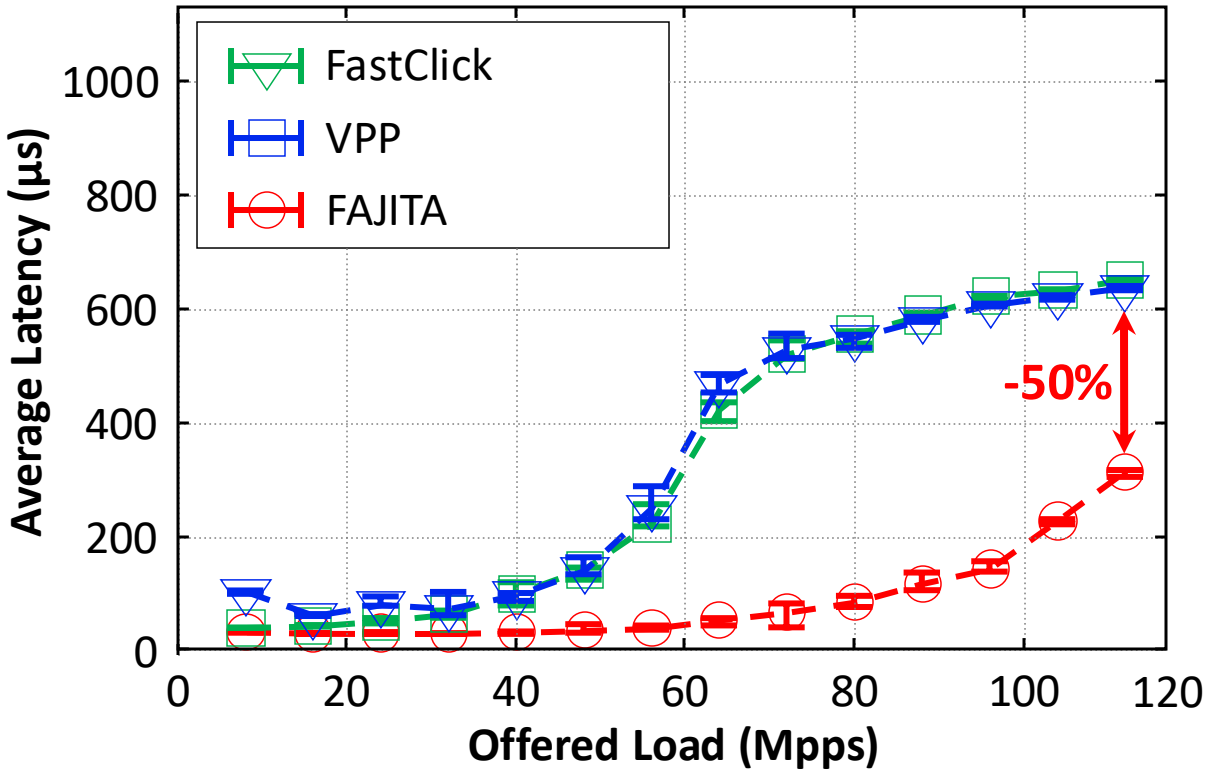


Evaluation

Does FAJITA Improve End-to-End Latency?



8 CPU cores

Load Balancer + Flow Statistics Counter

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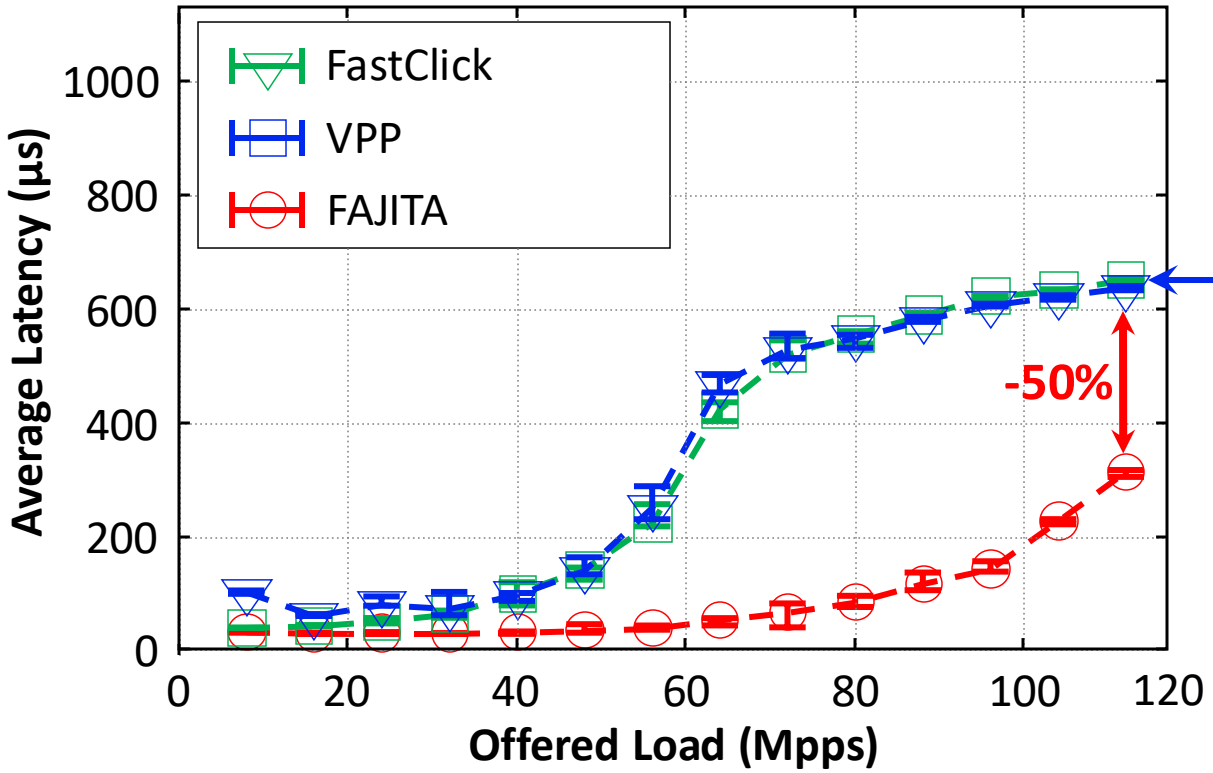


One of the three principles is **overlooked**

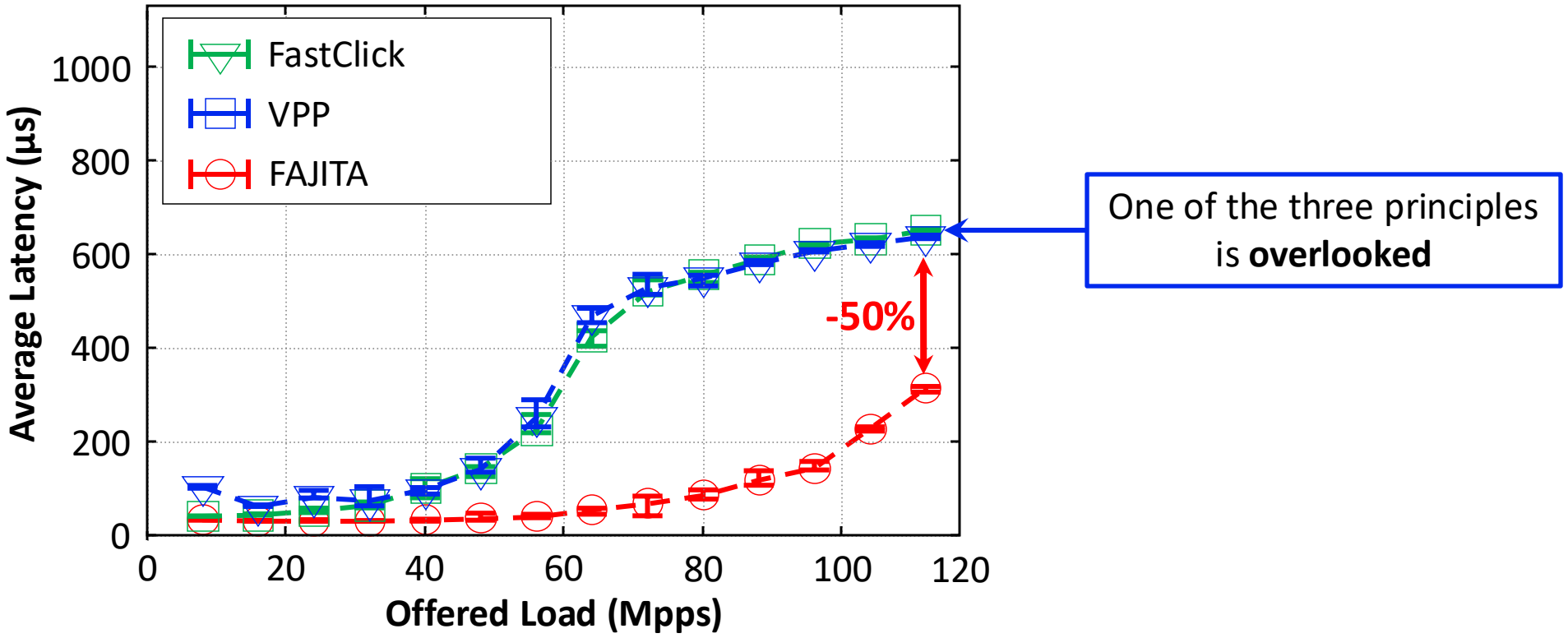
8 CPU cores

Load Balancer + Flow Statistics Counter

Evaluation

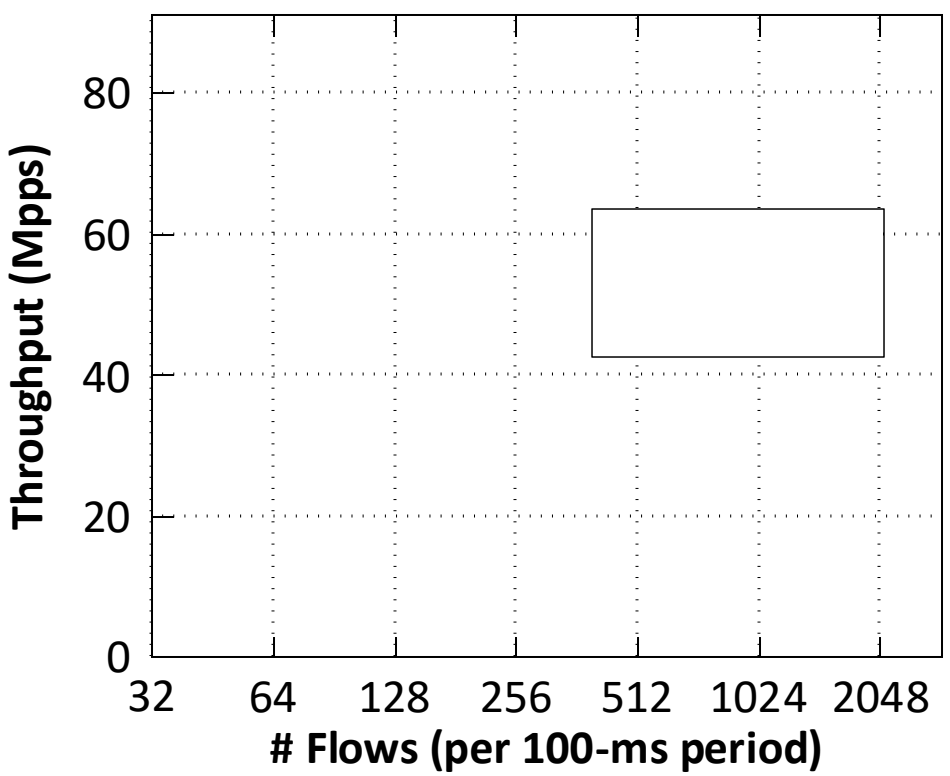
Does FAJITA Improve End-to-End Latency?

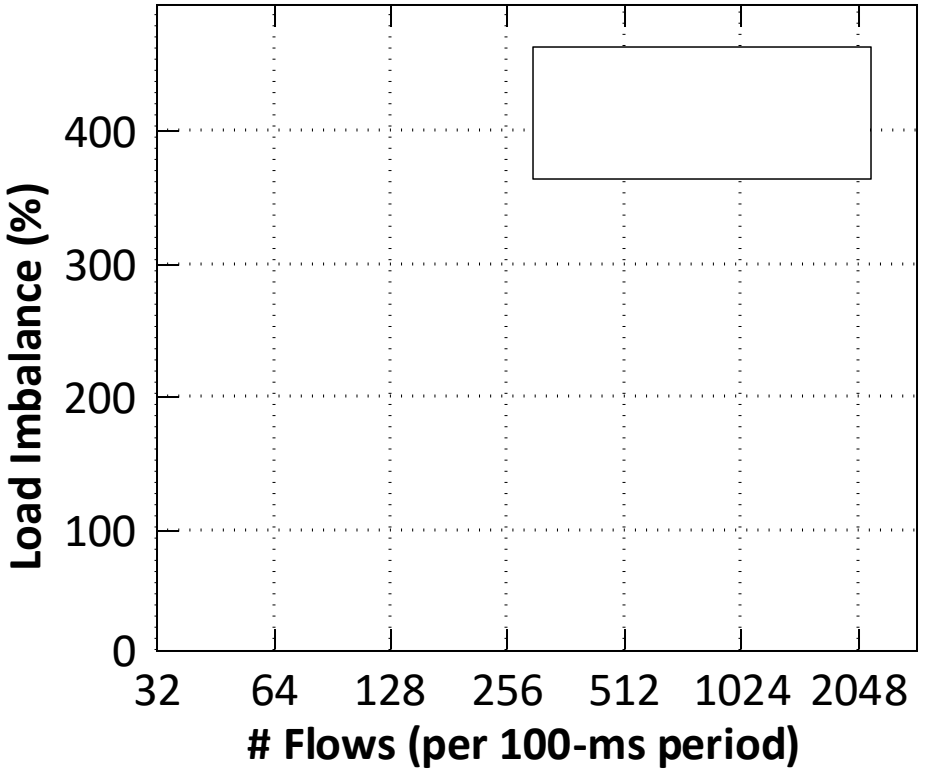
FAJITA performs stateful packet processing in **half the time** of other frameworks



Evaluation

Is RSS Sufficient for FAJITA?





8 CPU cores – Synthetic Trace w/ Elephants Only

Flow Statistics Counter – 100ms Monitoring Interval

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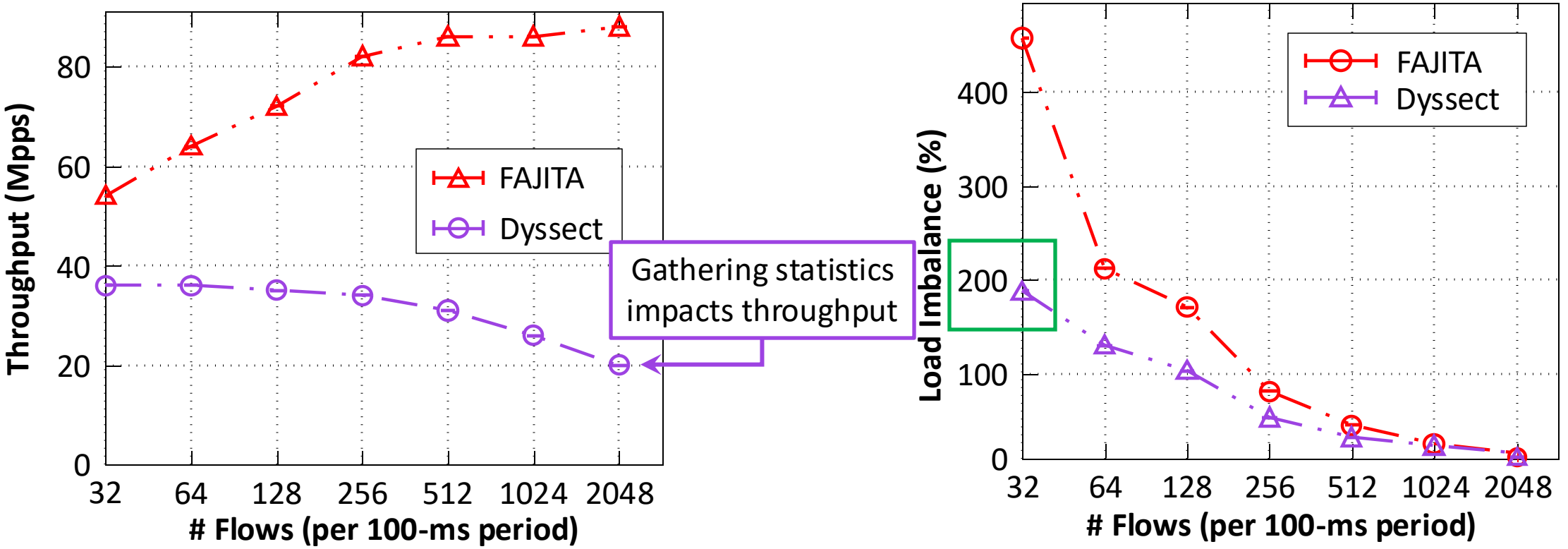

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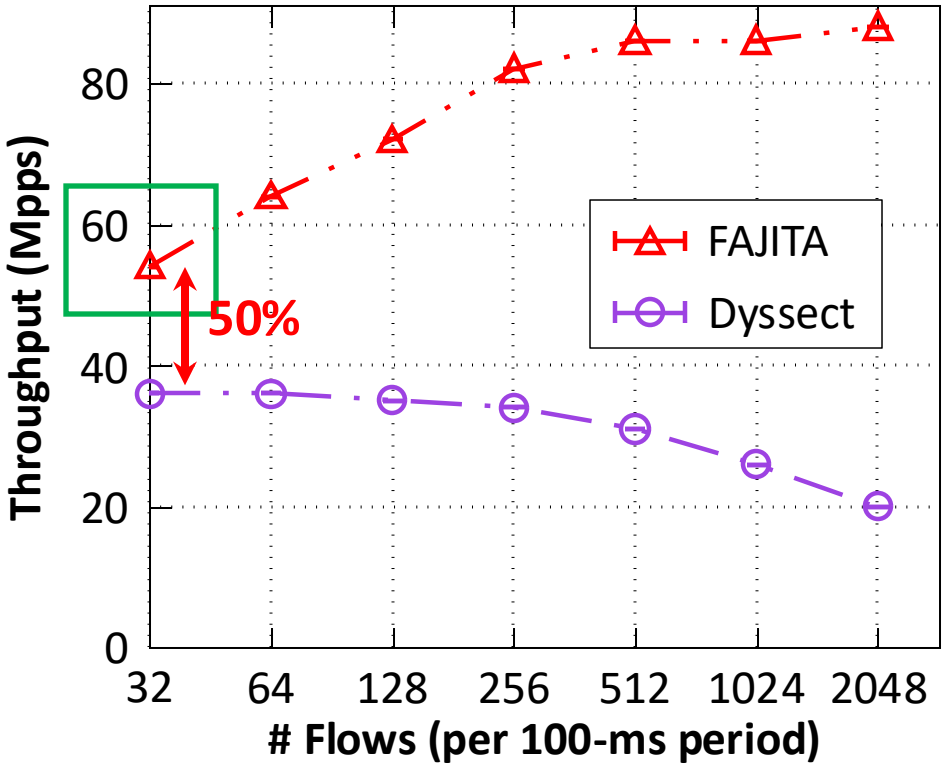

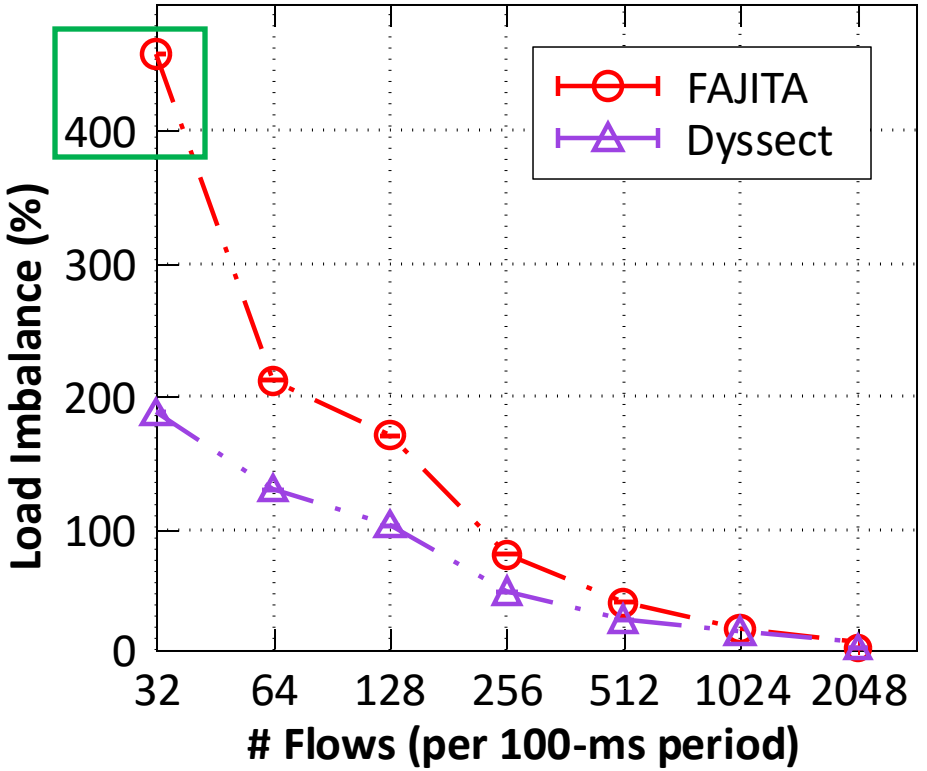

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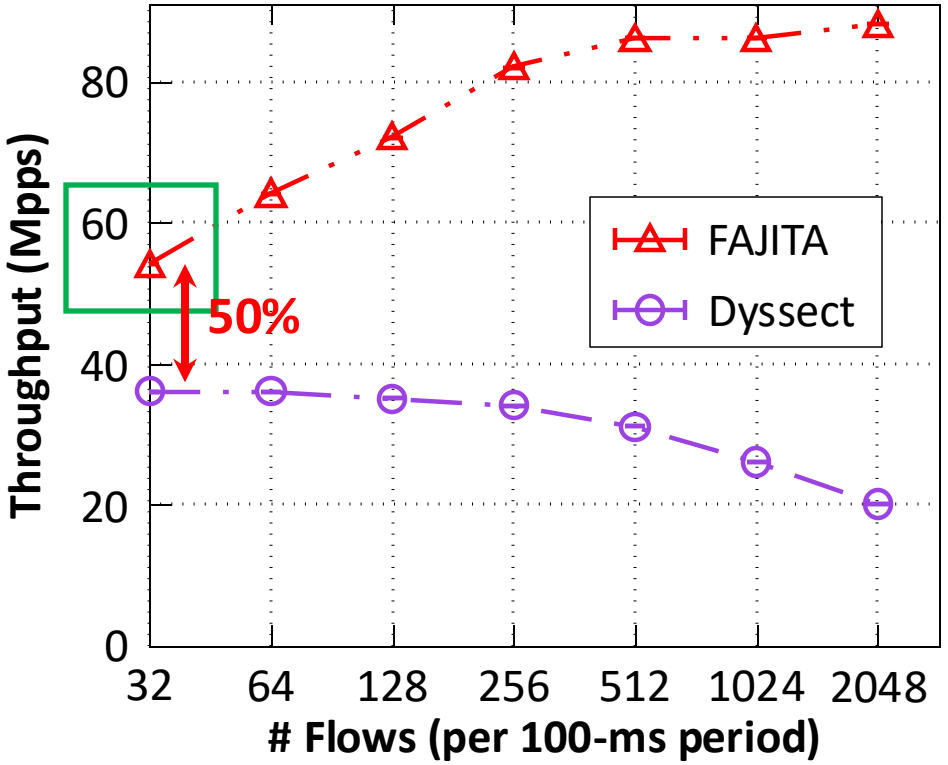
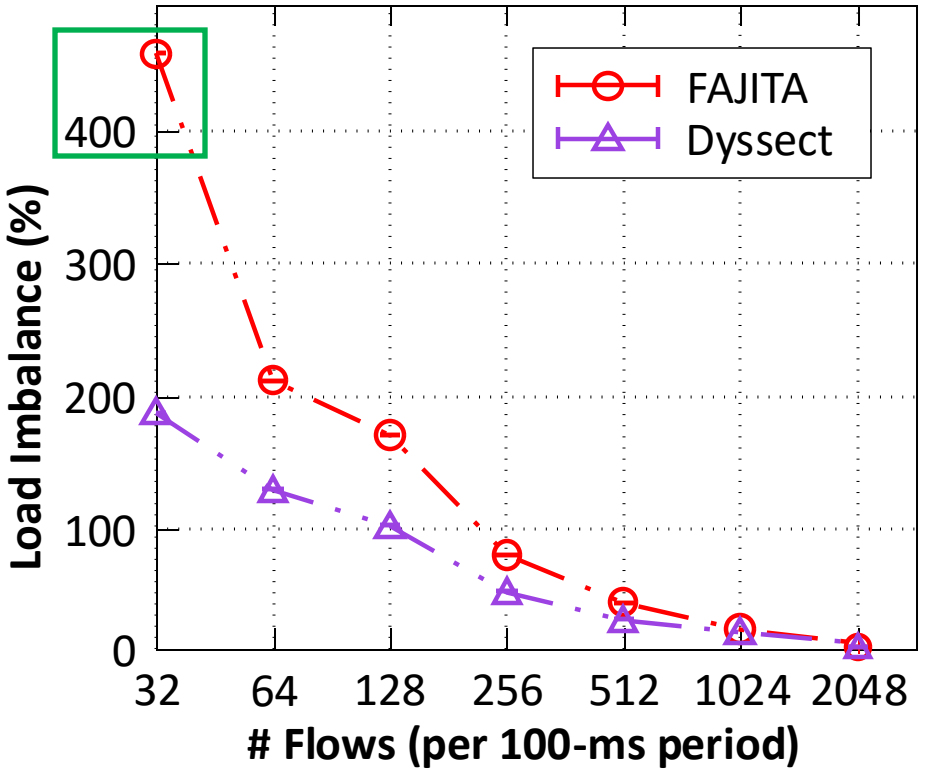
Evaluation

Is RSS Sufficient for FAJITA?

FAJITA achieves better performance **solely relying on RSS**

Load imbalance **only** depends on the number of flows, that are usually **>2K at high rates**!





FAJITA take-away

The **FAJITA** system:

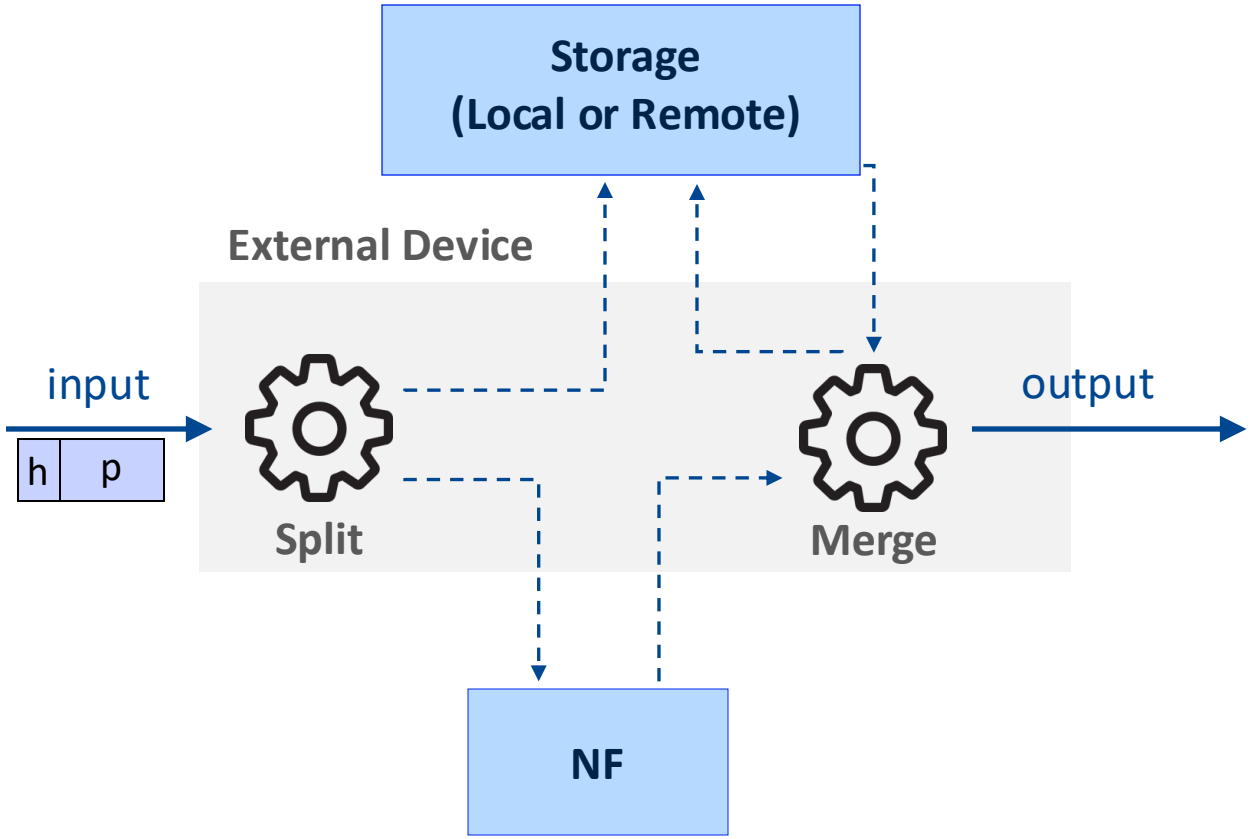
- **incorporates** the three essential principles for stateful packet processing **together**
- **minimizes** memory access overheads by **exploiting batching** & **software prefetching**
- **alleviates** overheads of accessing shared data structures **by introducing auxiliary HTs**
- achieves **performance 2x higher** than existing stateful packet processors
- demonstrates that dynamic inter-core load balancing is **detrimental** at high rates
- only processes packet headers

How to split packets?

How to split packets?

State-of-the-art **packet-splitting** solutions **increase** shallow NFs throughput

e.g., Ribosome, nicmem



Packet-Splitting Approaches

State-of-the-art packet-splitting solutions increase NFs throughput

Improve NF Performance

Better CPU cache exploitation

Free up Bandwidth

Reduce the number of dedicated NF servers

Lower energy consumption

Complex Deployment

Require end-host modifications

Require available shared resources

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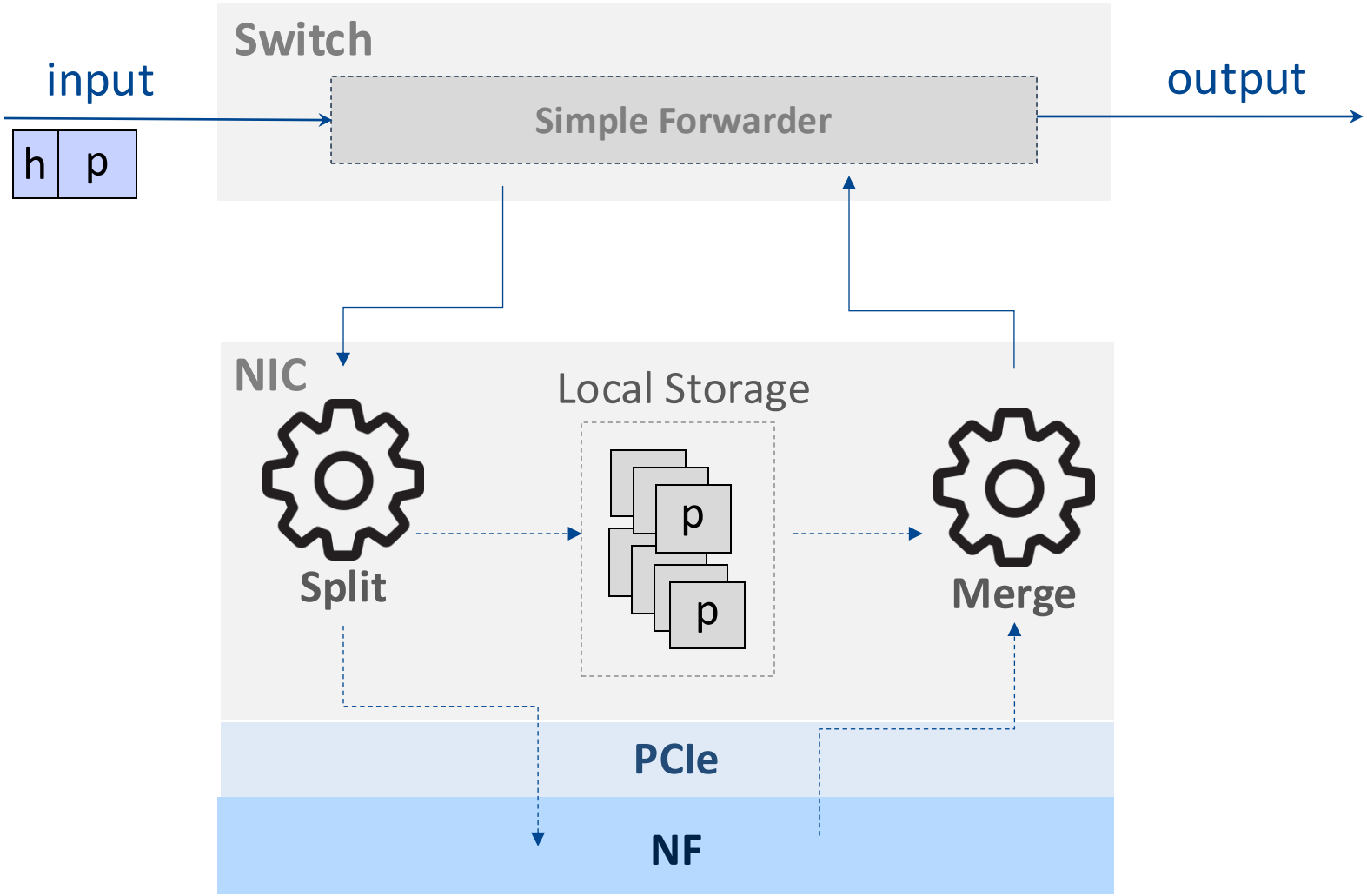

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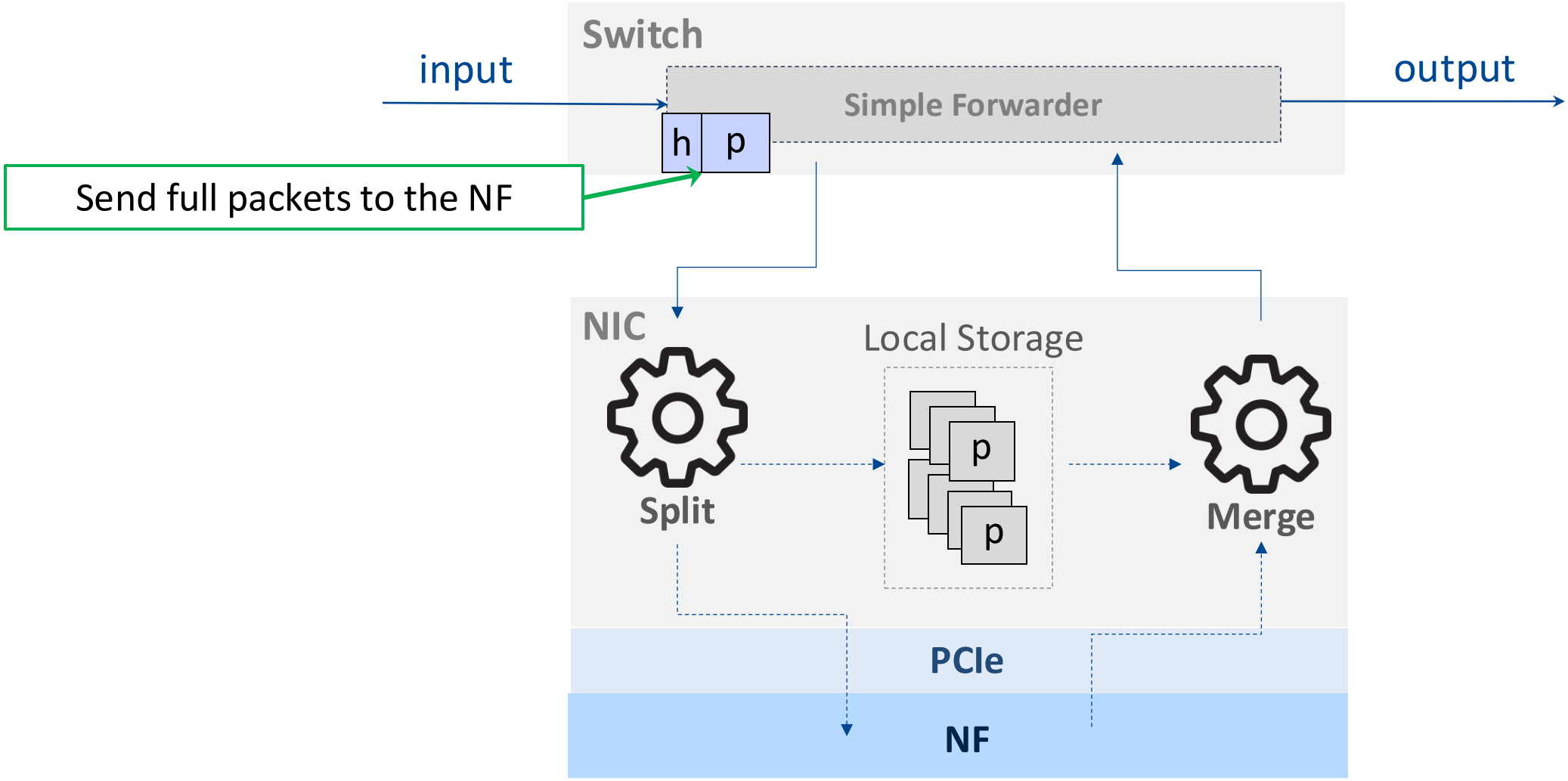

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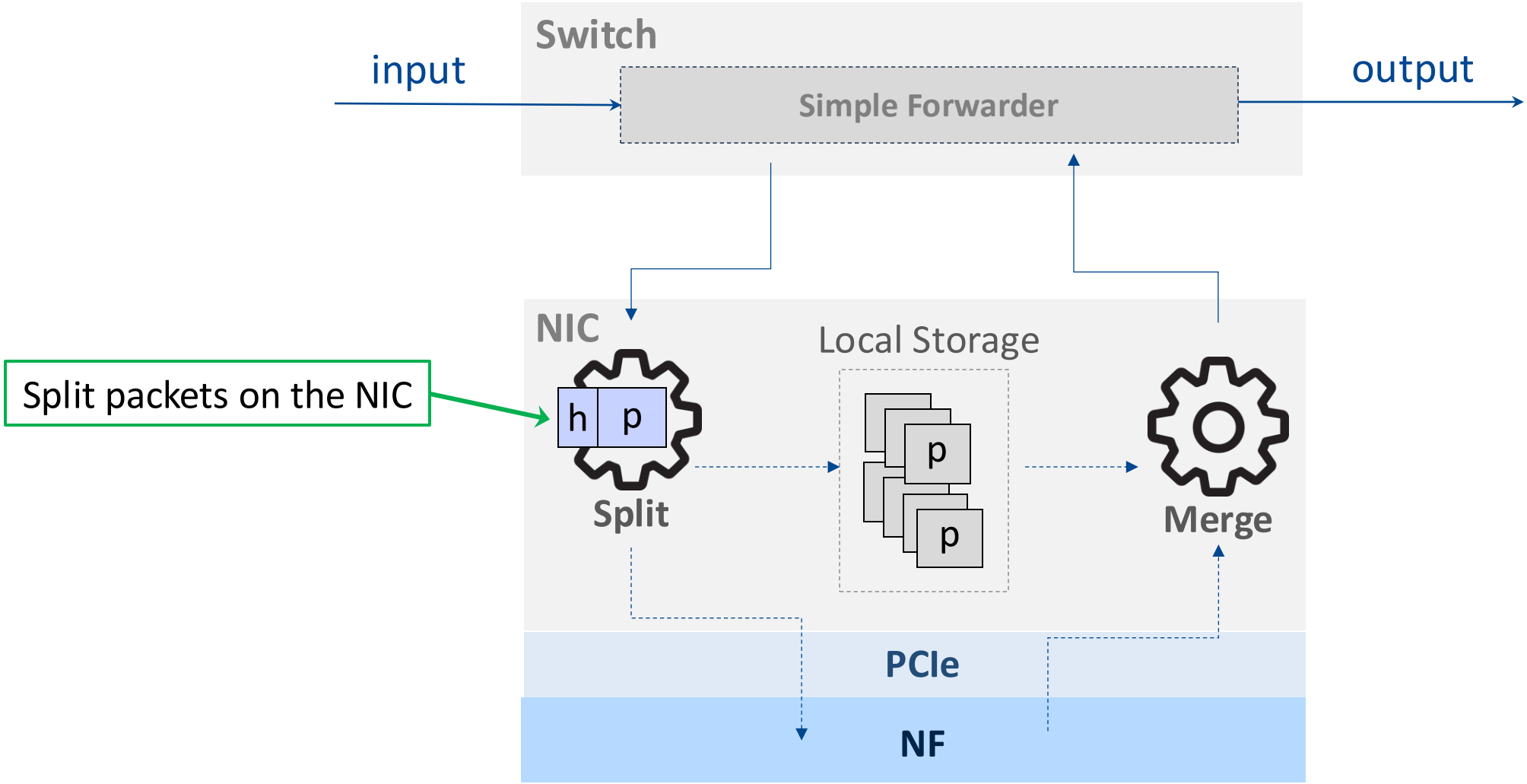

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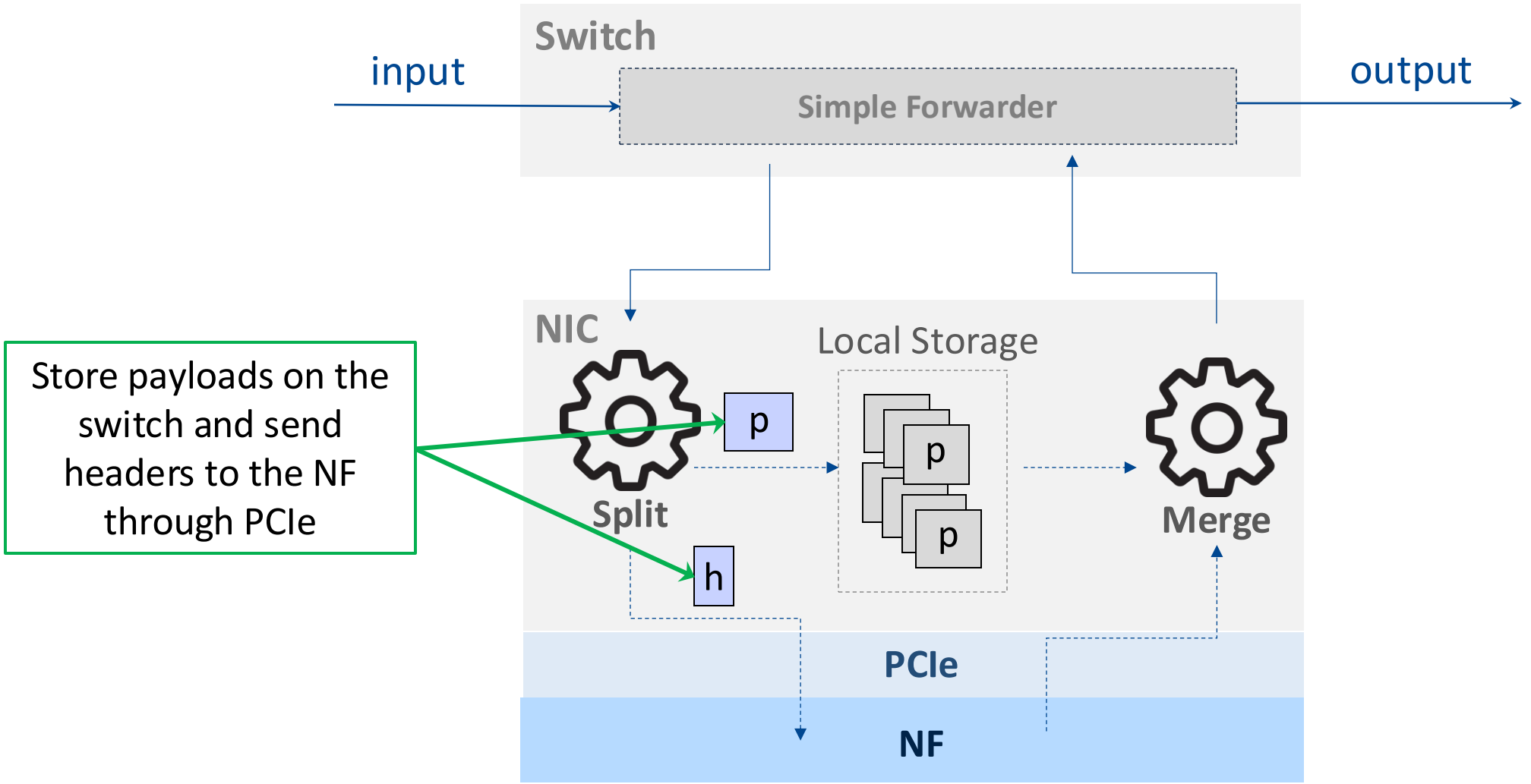

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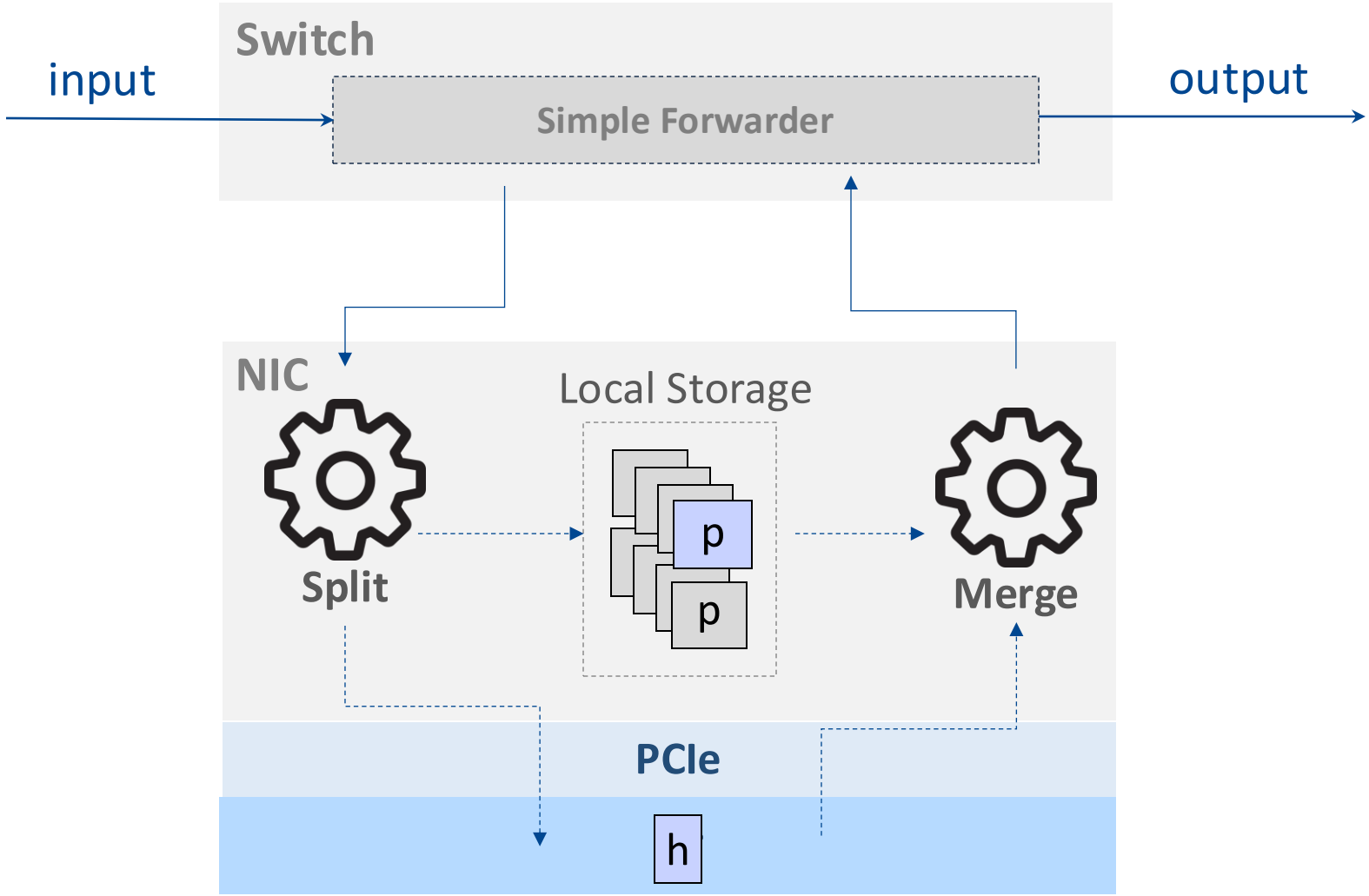

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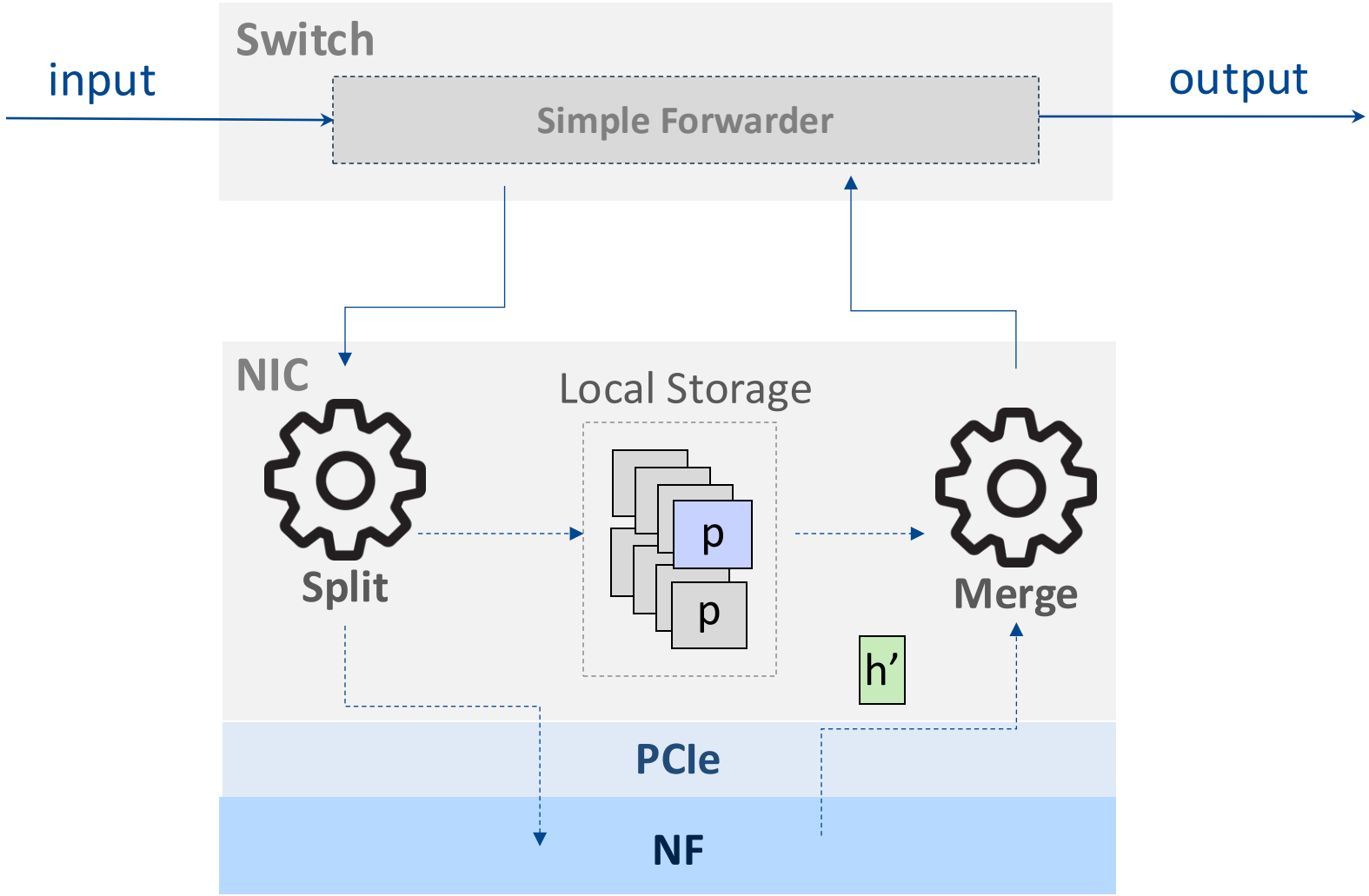

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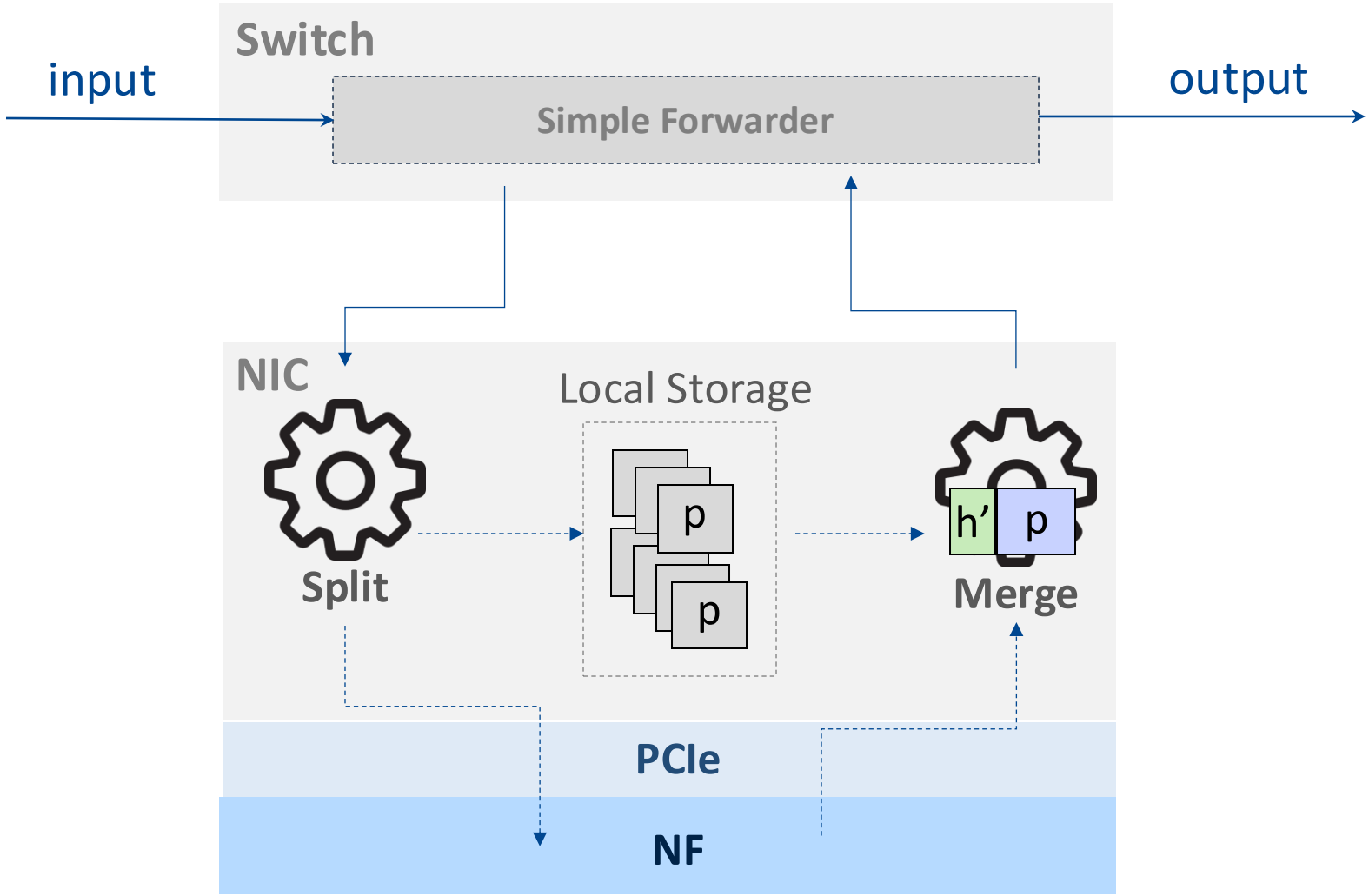

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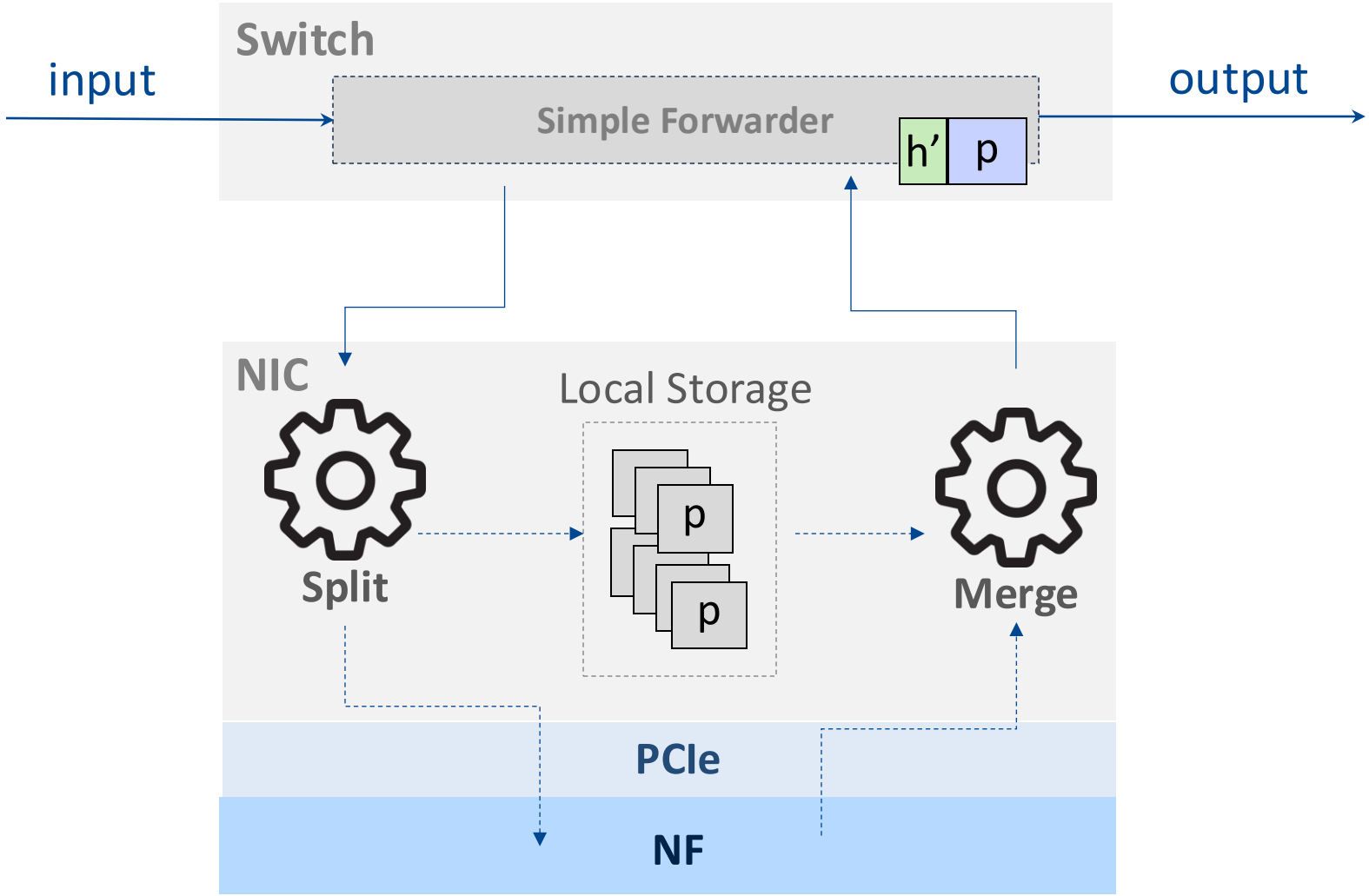

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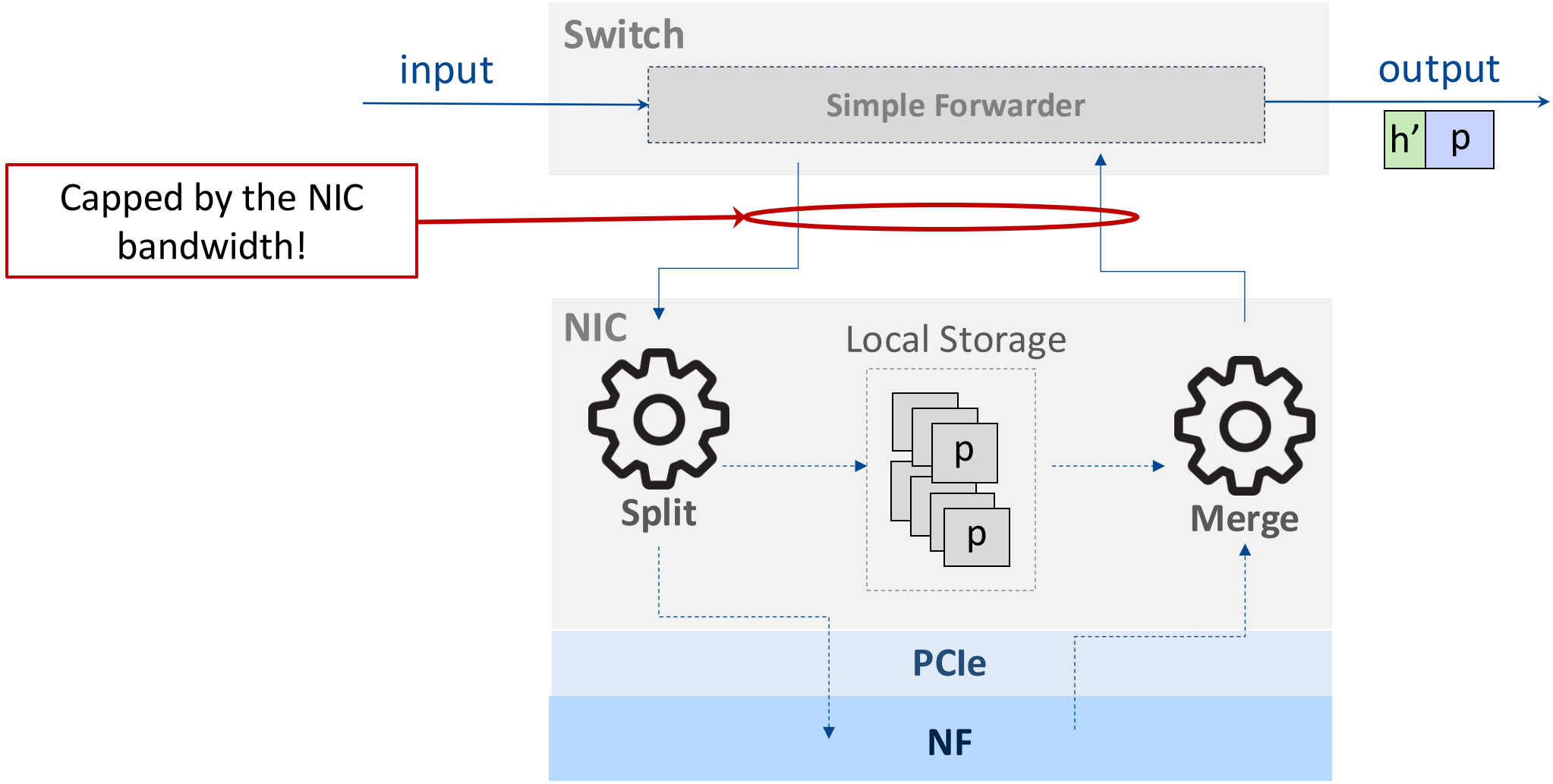

Packet-Splitting Approaches

State-of-the-art packet-splitting solutions increase NFs throughput

Storing Payloads in the On-NIC Memory (nicmem) 

Storing Payloads on Shared Resources (Ribosome) 

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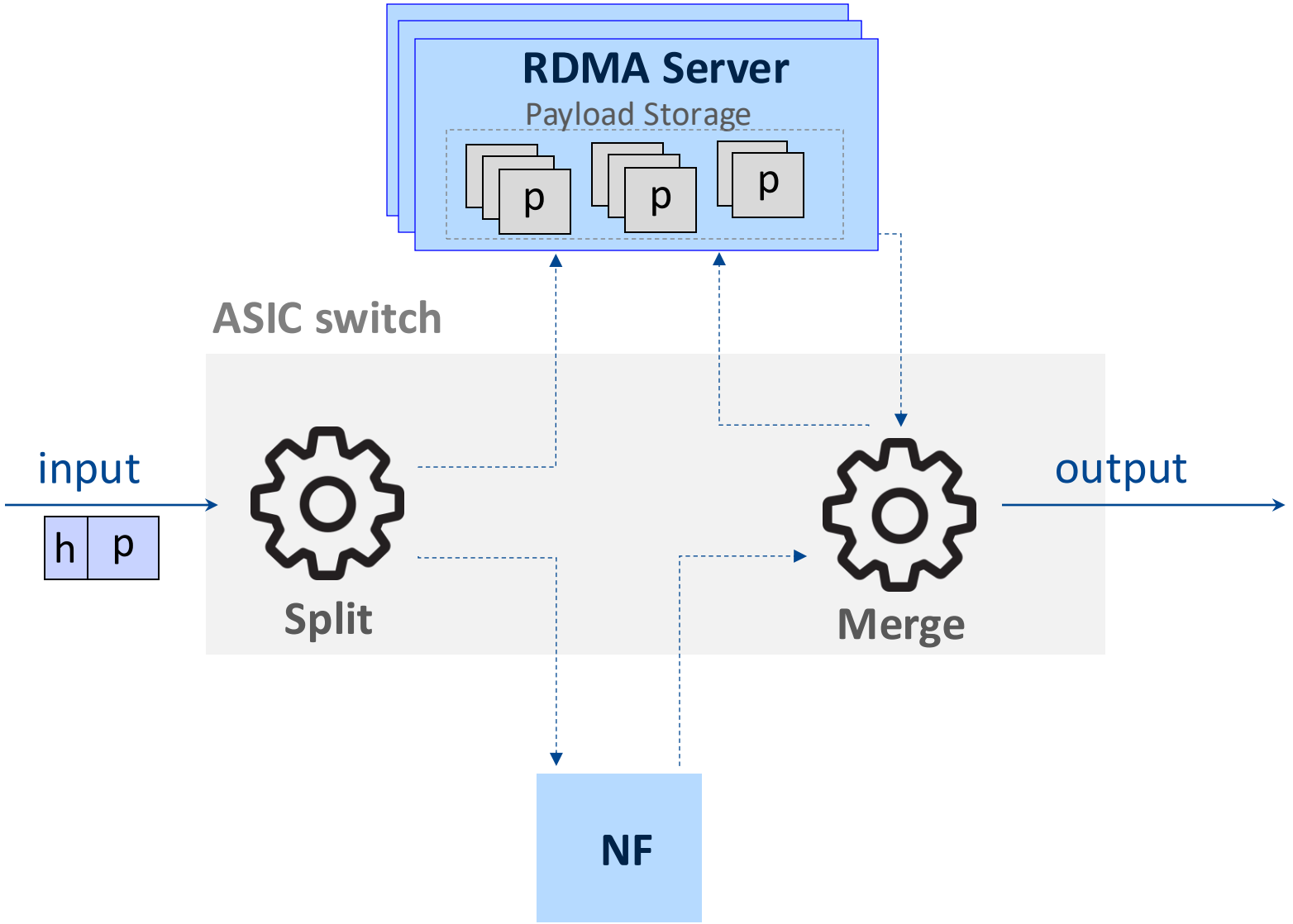

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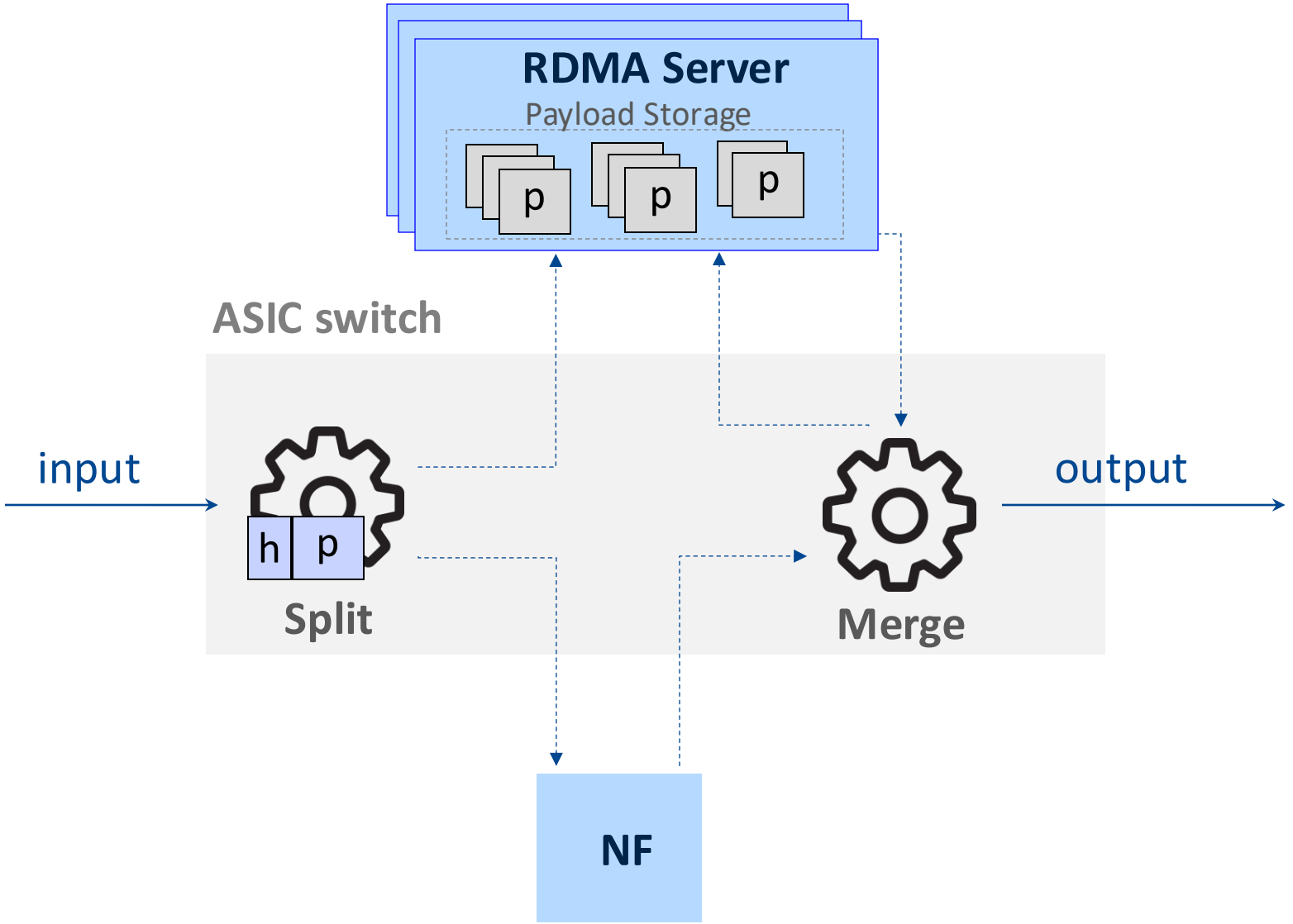

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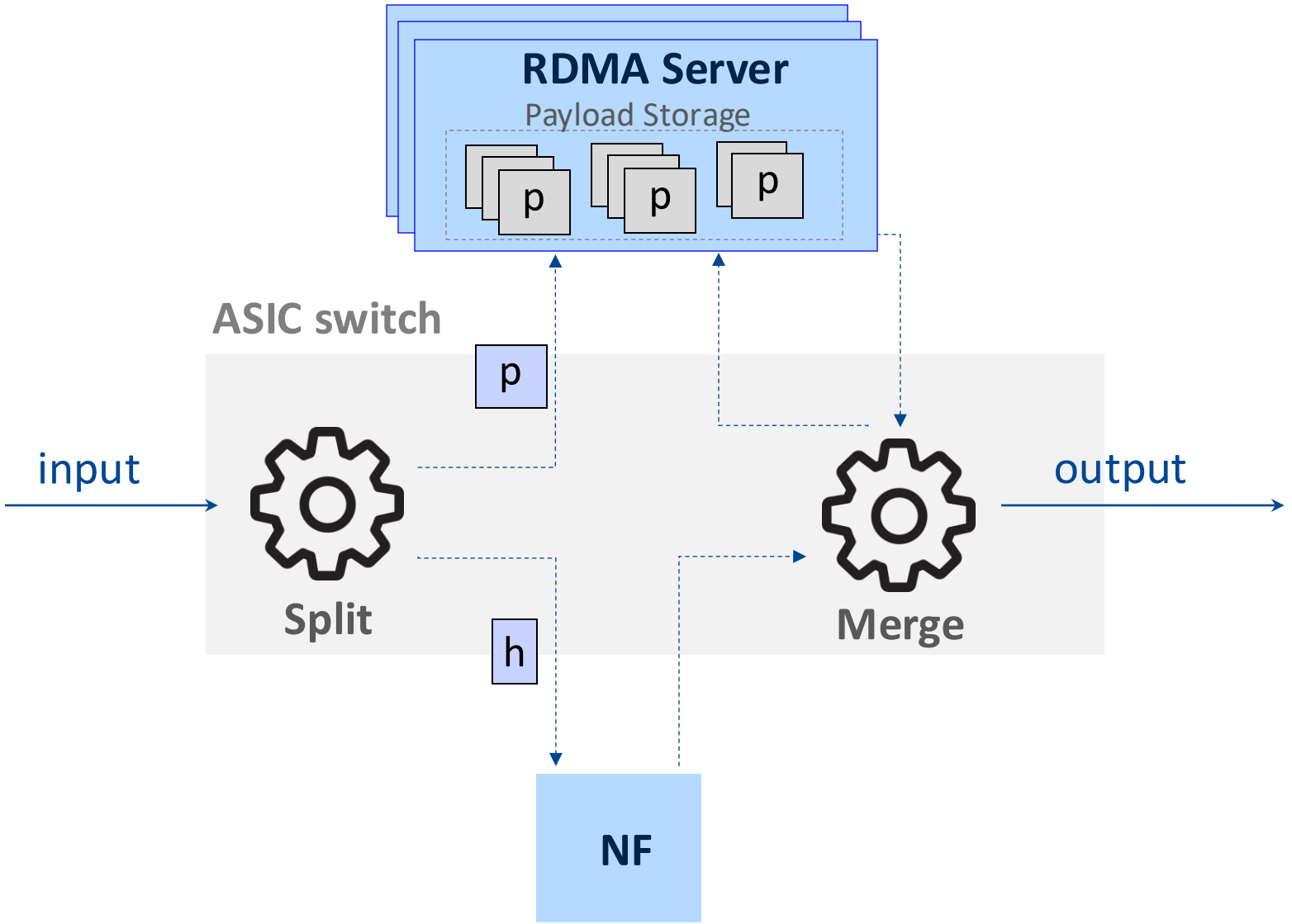

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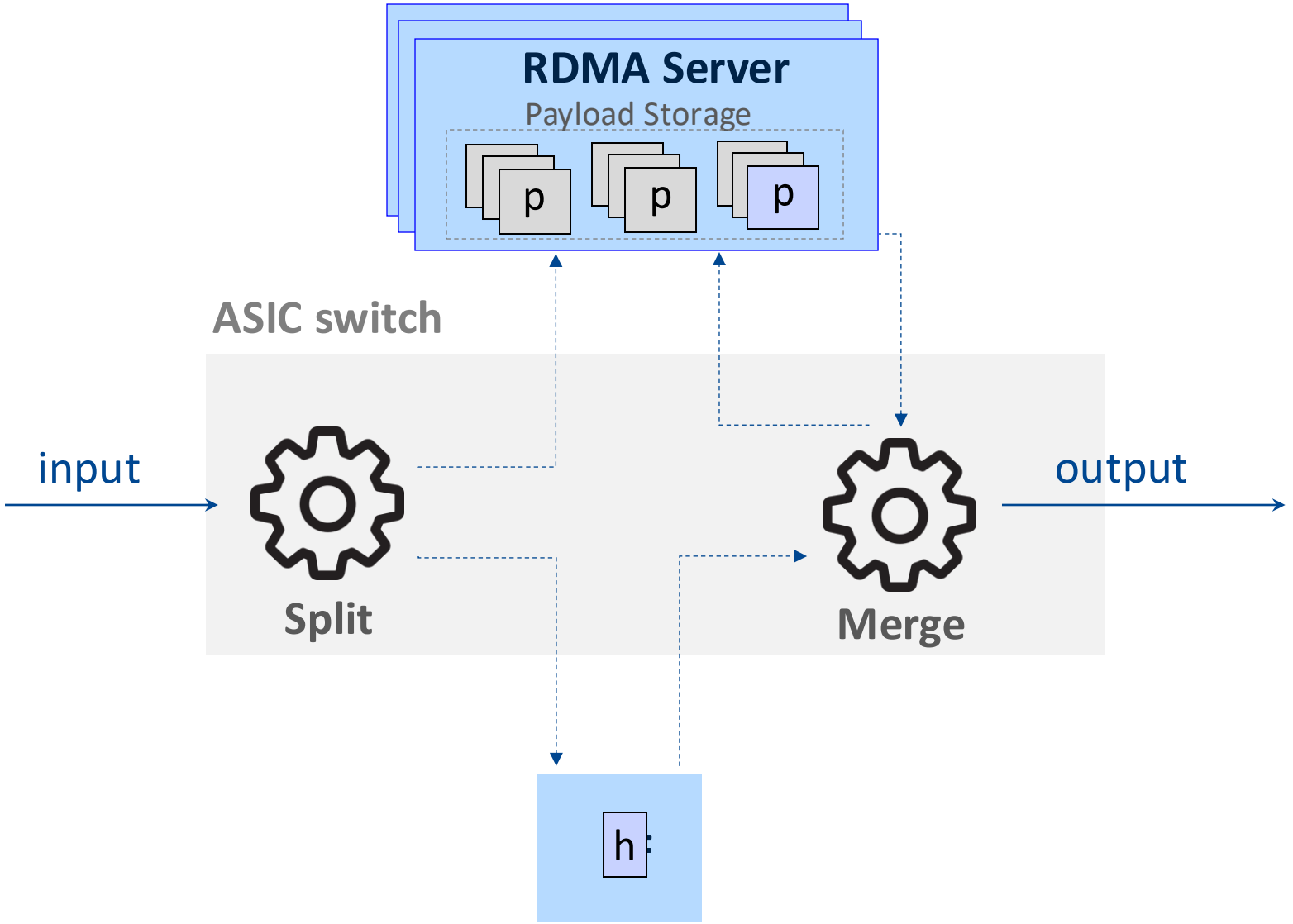

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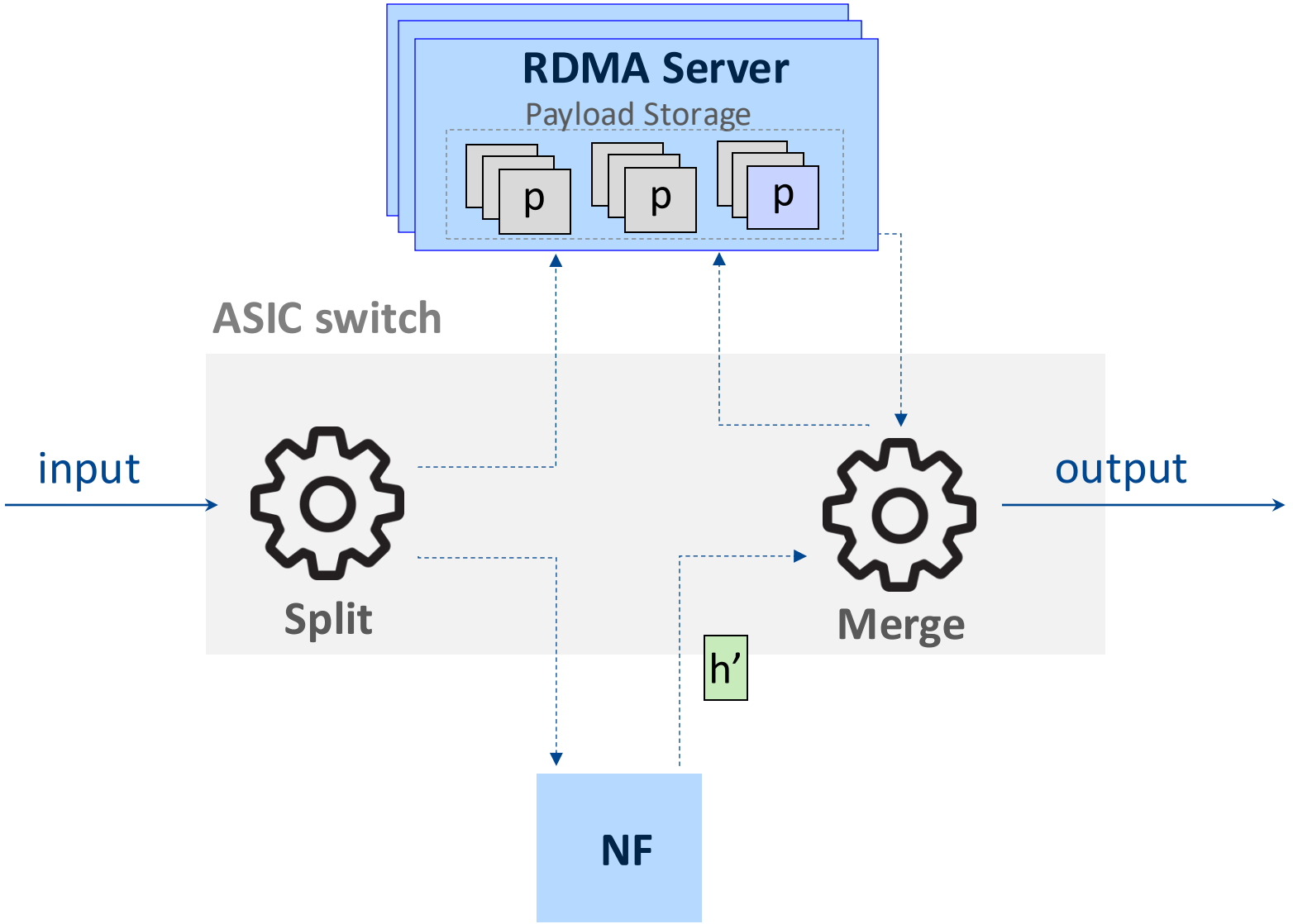

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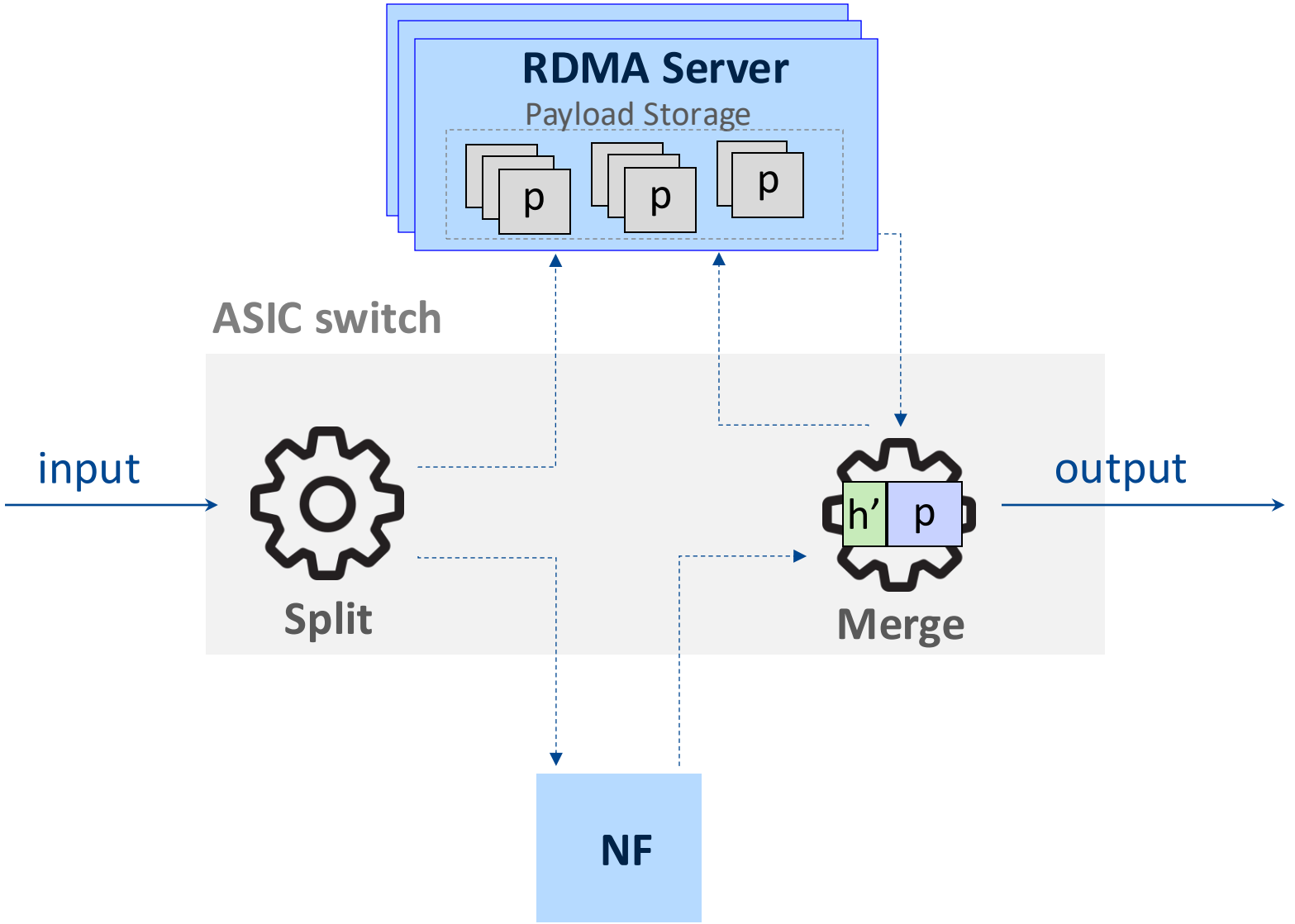
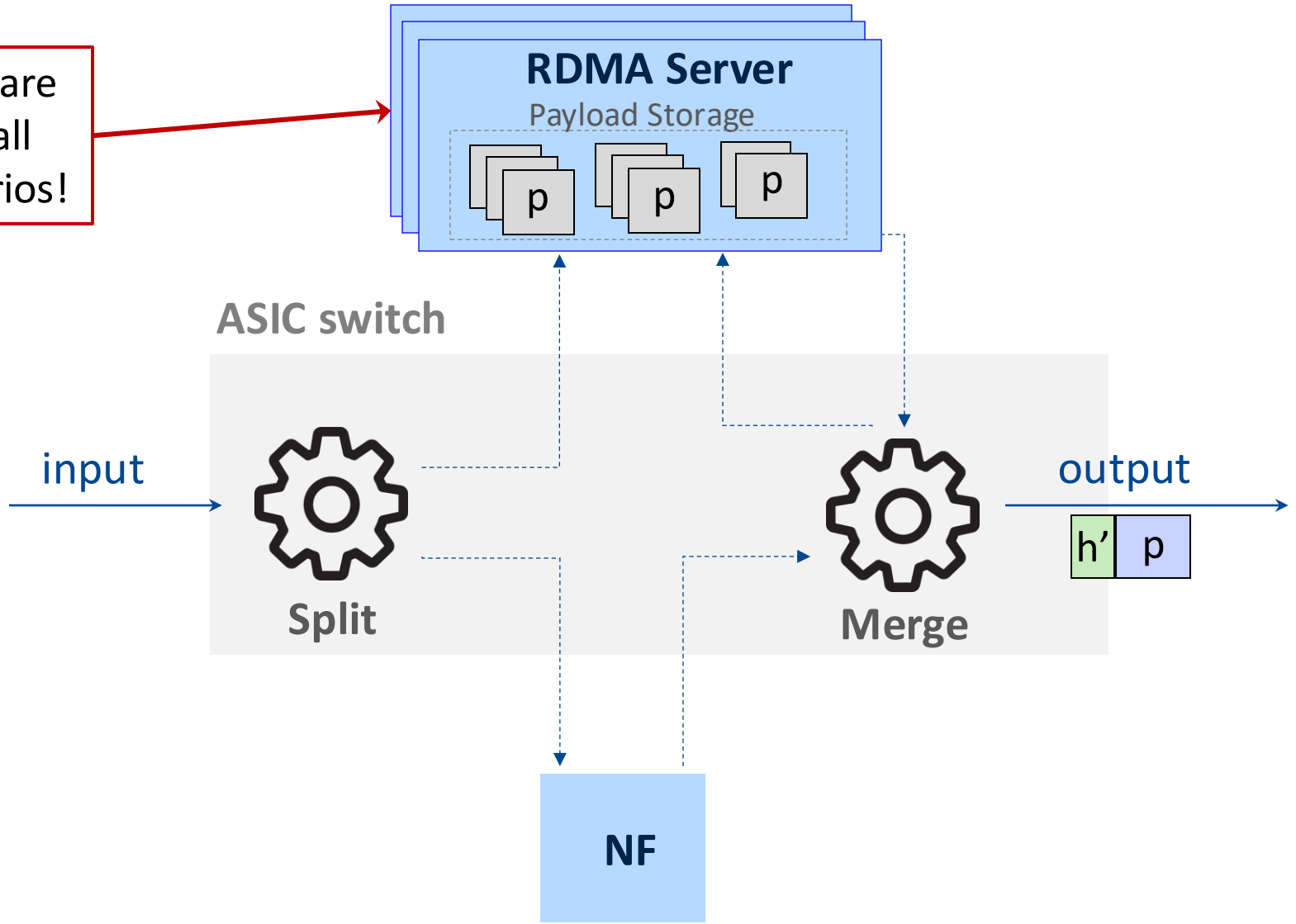


Storing Payloads on Shared Resources (Ribosome)

Shared resources are not available in all operational scenarios!



Packet-Splitting Approaches

State-of-the-art packet-splitting solutions increase NFs throughput

Storing Payloads in the On-NIC Memory (nicmem) 

Storing Payloads on Shared Resources (Ribosome) 

Store on the ASIC SRAM

- ideal, but how? no API to store payloads!

Can we store the entire payload within the switch without requiring external devices?

Core Idea: A Queue-Based Packet Storage

Exploit the switch shared buffer to store payloads

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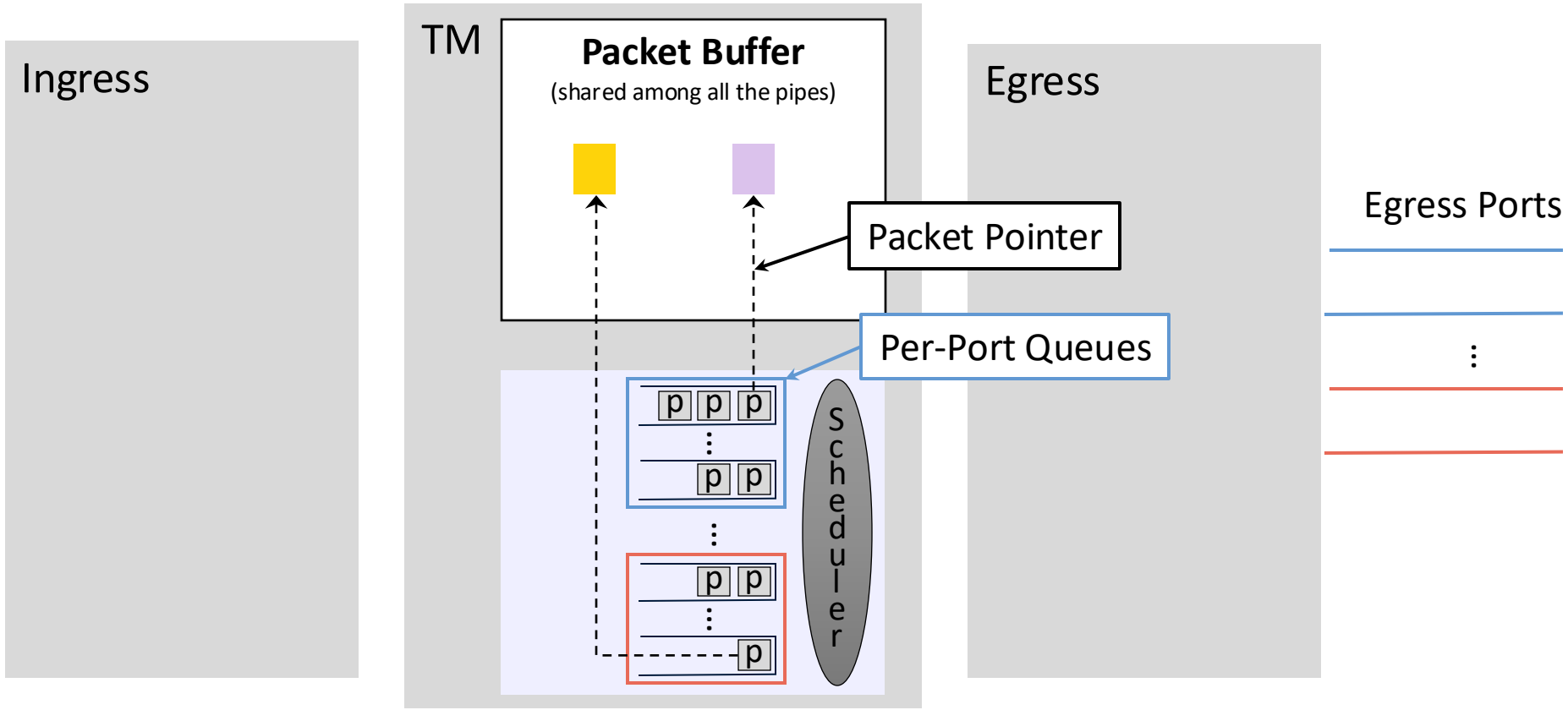
Exploit the switch shared buffer to store payloads



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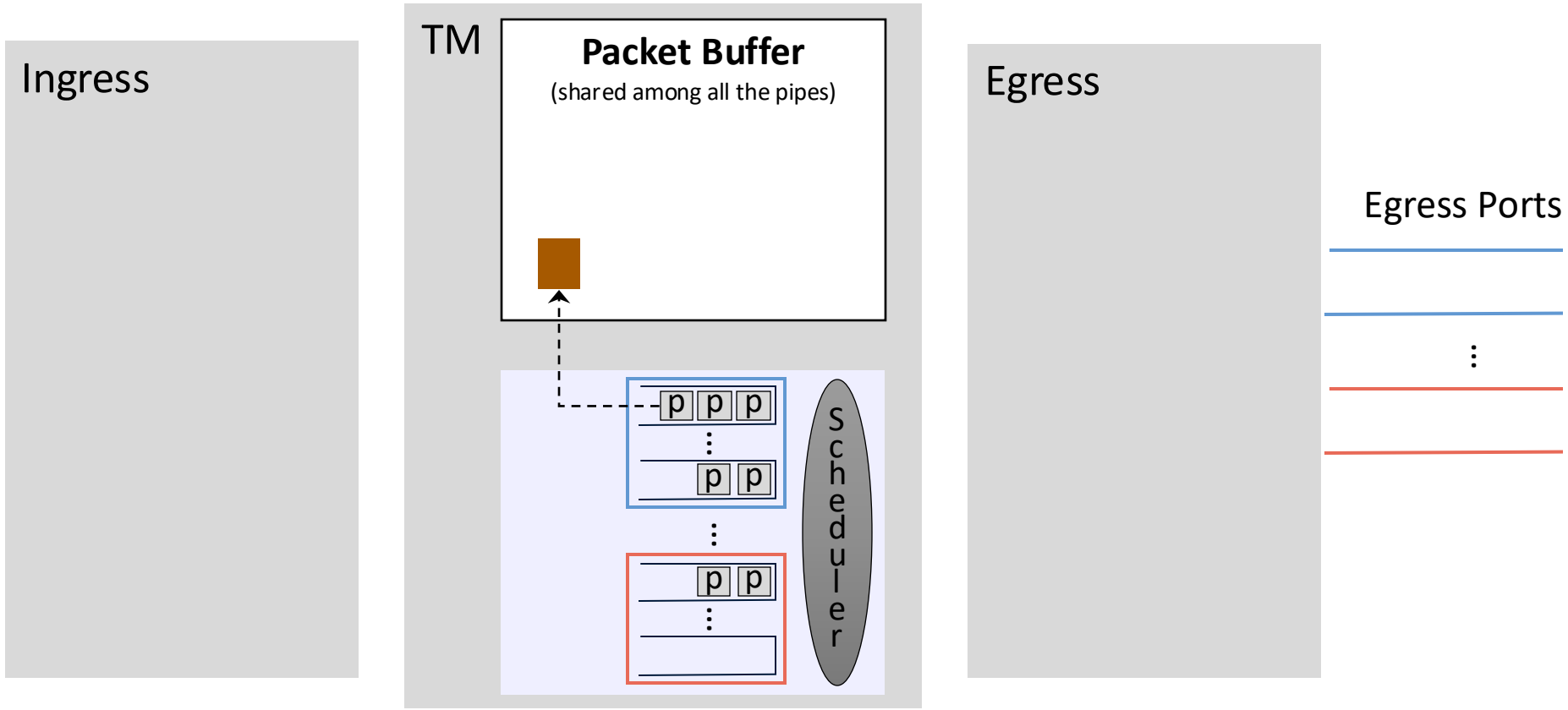


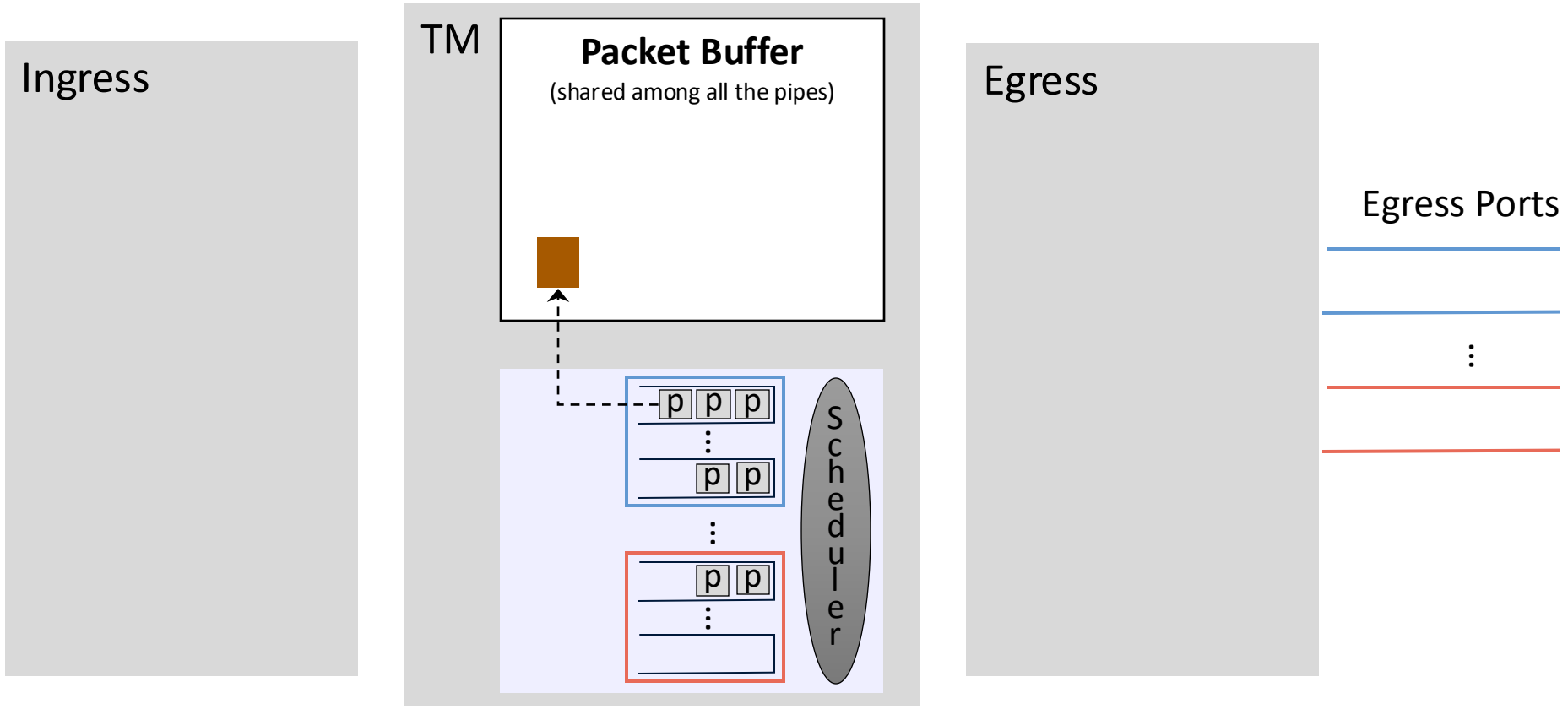
Core Idea: A Queue-Based Packet Storage

Exploit the switch shared buffer to store payloads

✓ Large shared buffer

✗ No programmatic access

? How can we access the packet buffer?



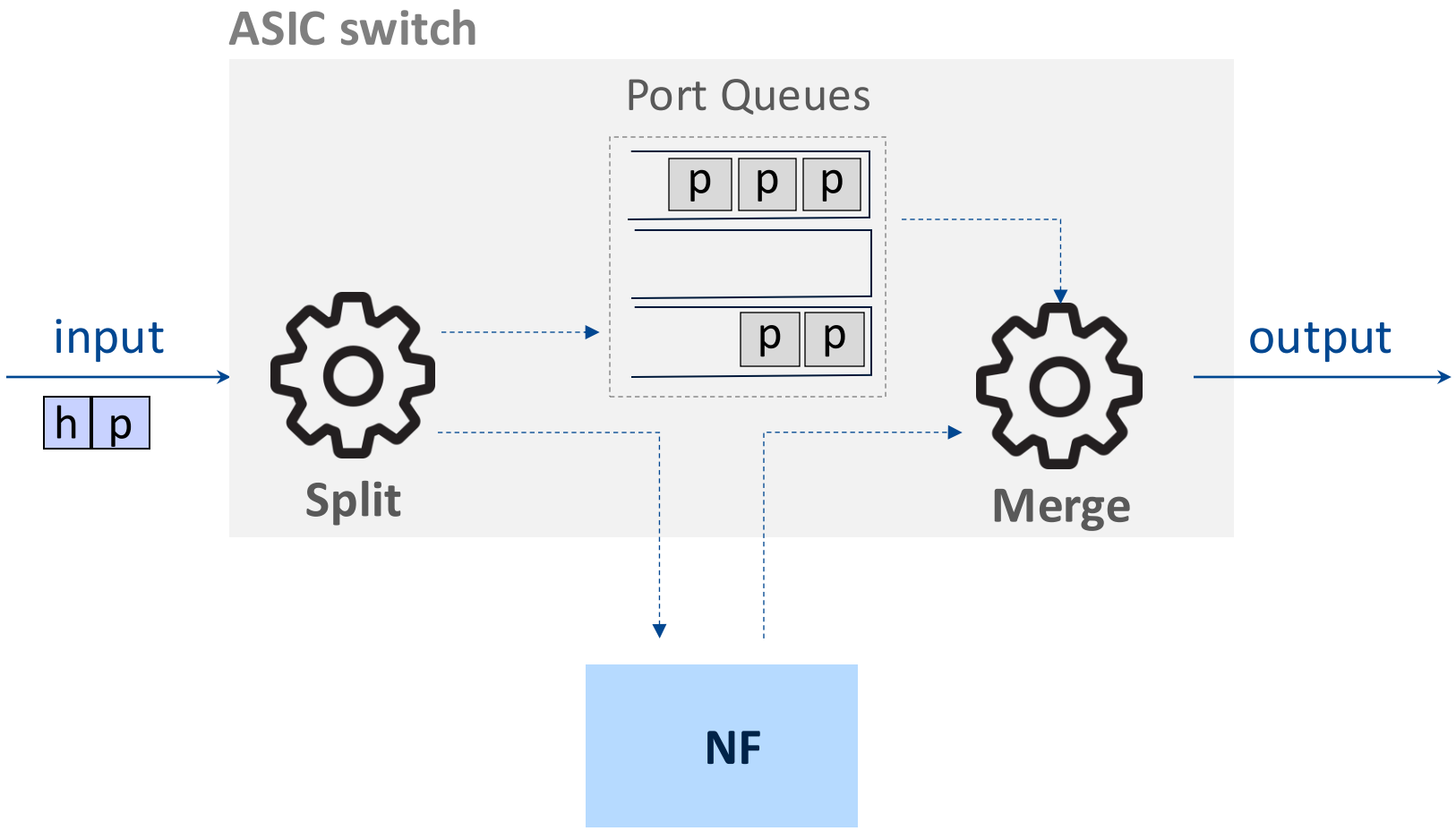
How can we access the packet buffer?

Enqueued packets **implicitly** control the buffer memory

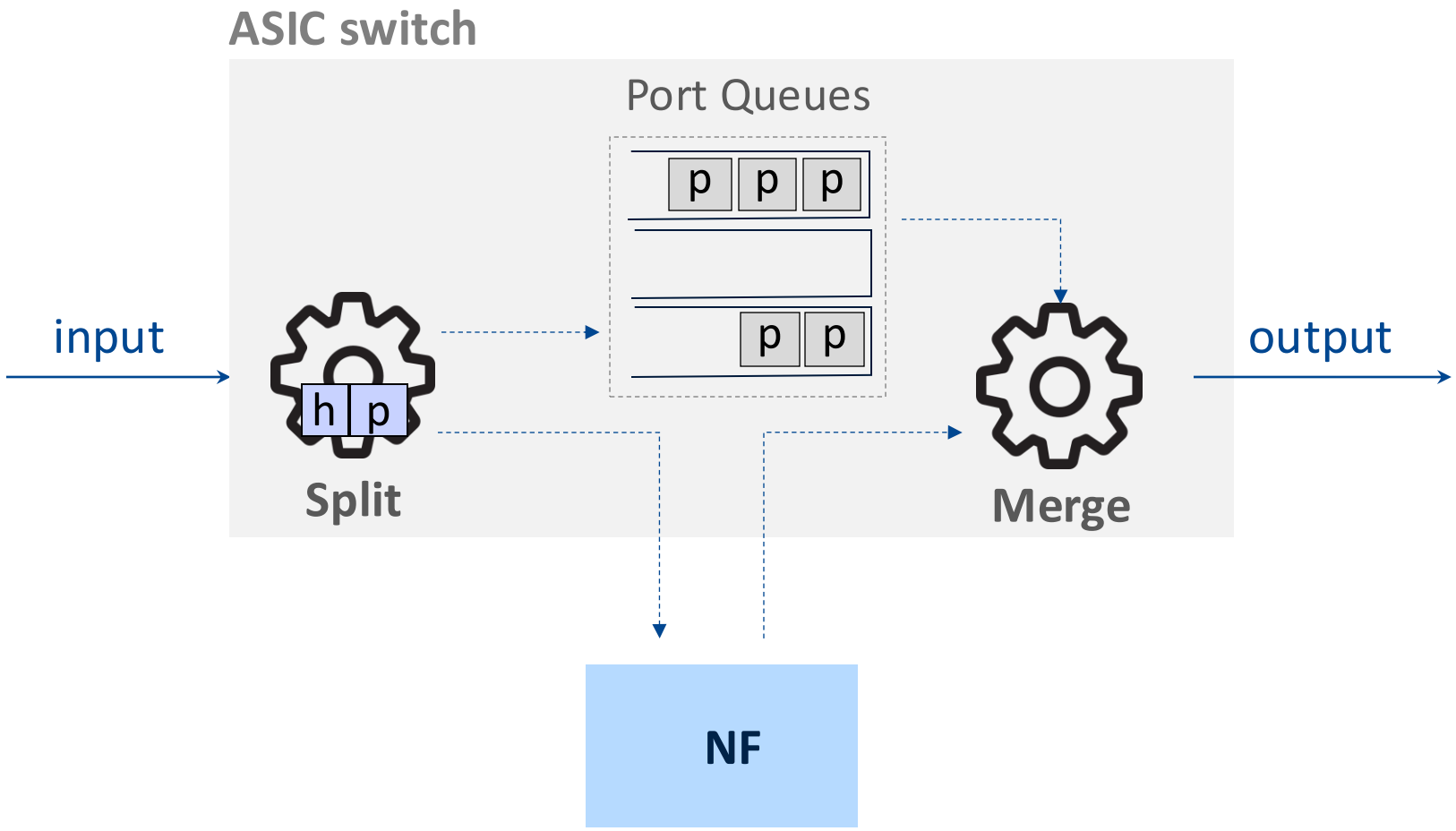
Hold payloads in the port queues until
the processed header from the NF is returned!

Would it work for real?

Challenges


ASIC switch
Port Queues
p
p
p
p
p
input
h
p
Split
Merge
output
NF

Challenges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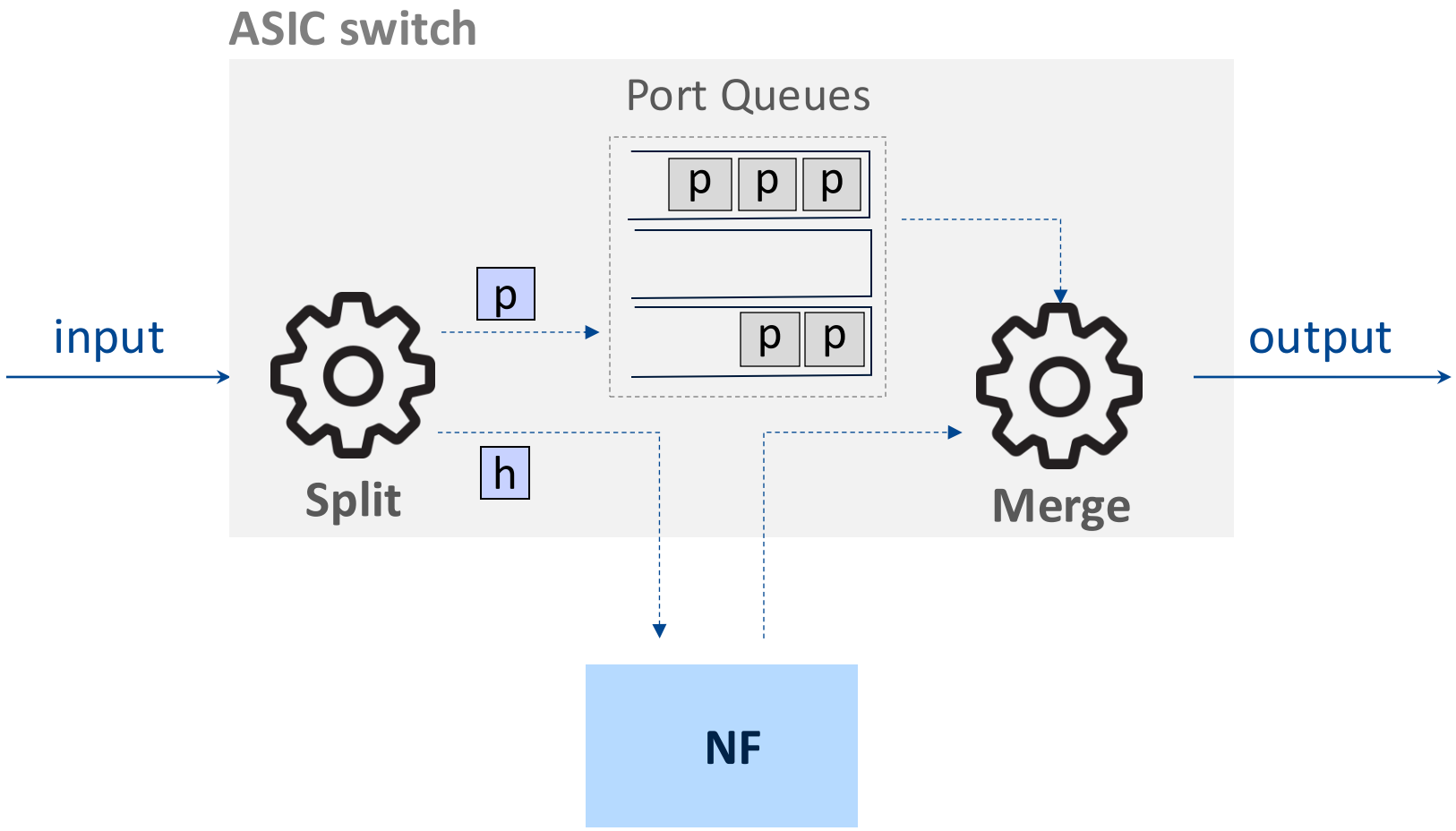
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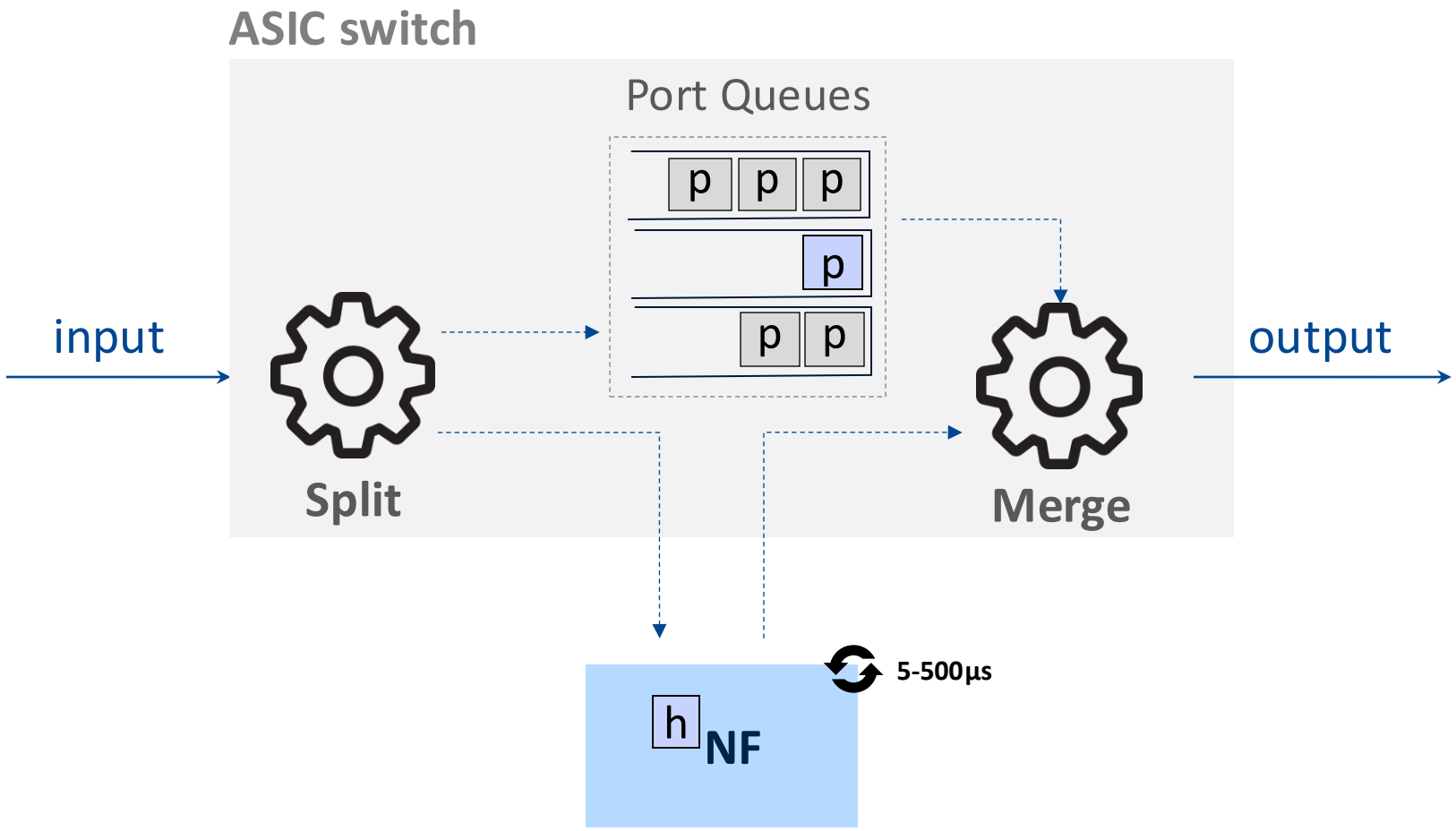
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Split
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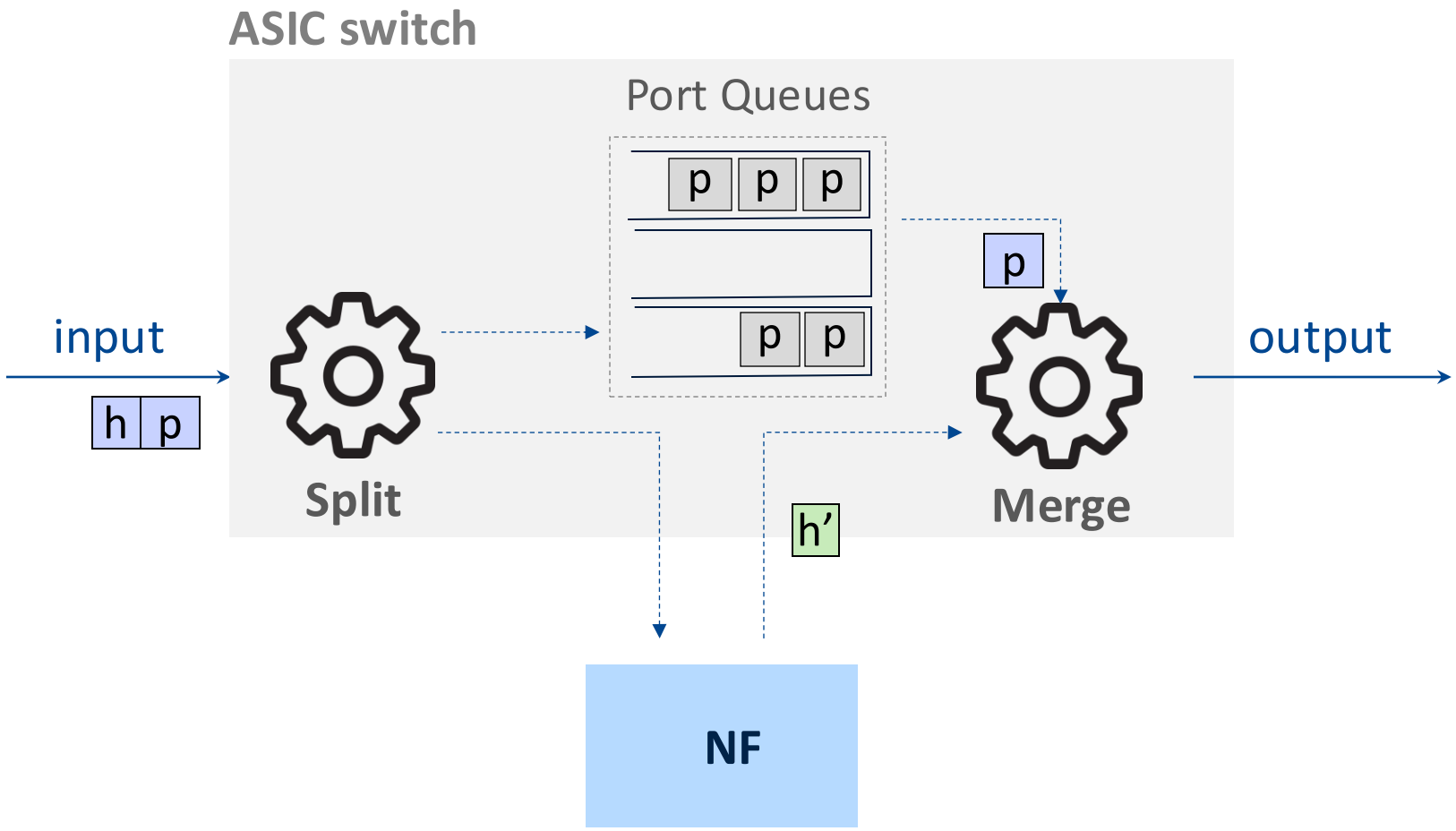
h
NF
5-500µs

Challenges


ASIC switch
Port Queues
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p
input
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p
Split
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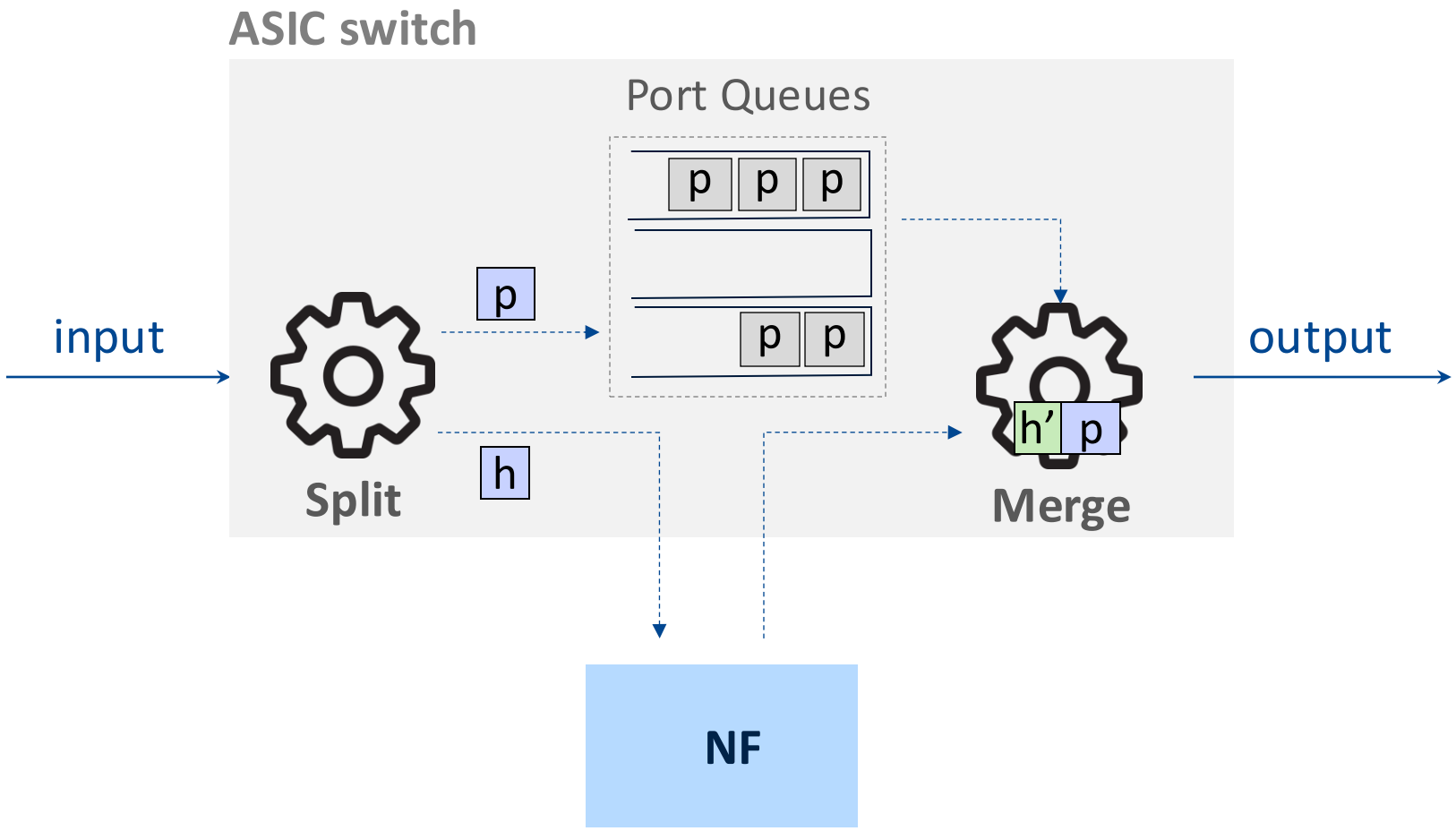
Challenges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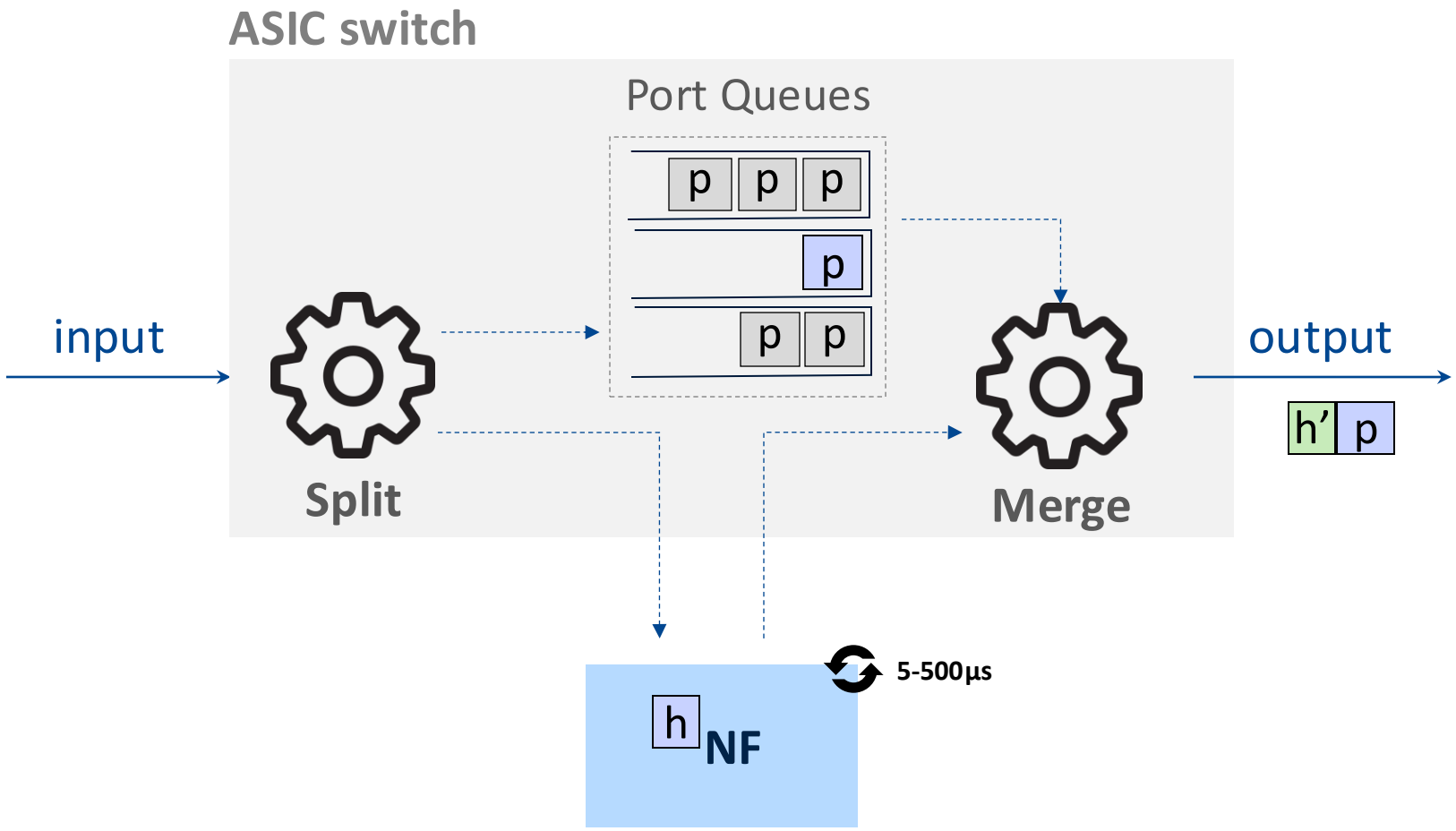
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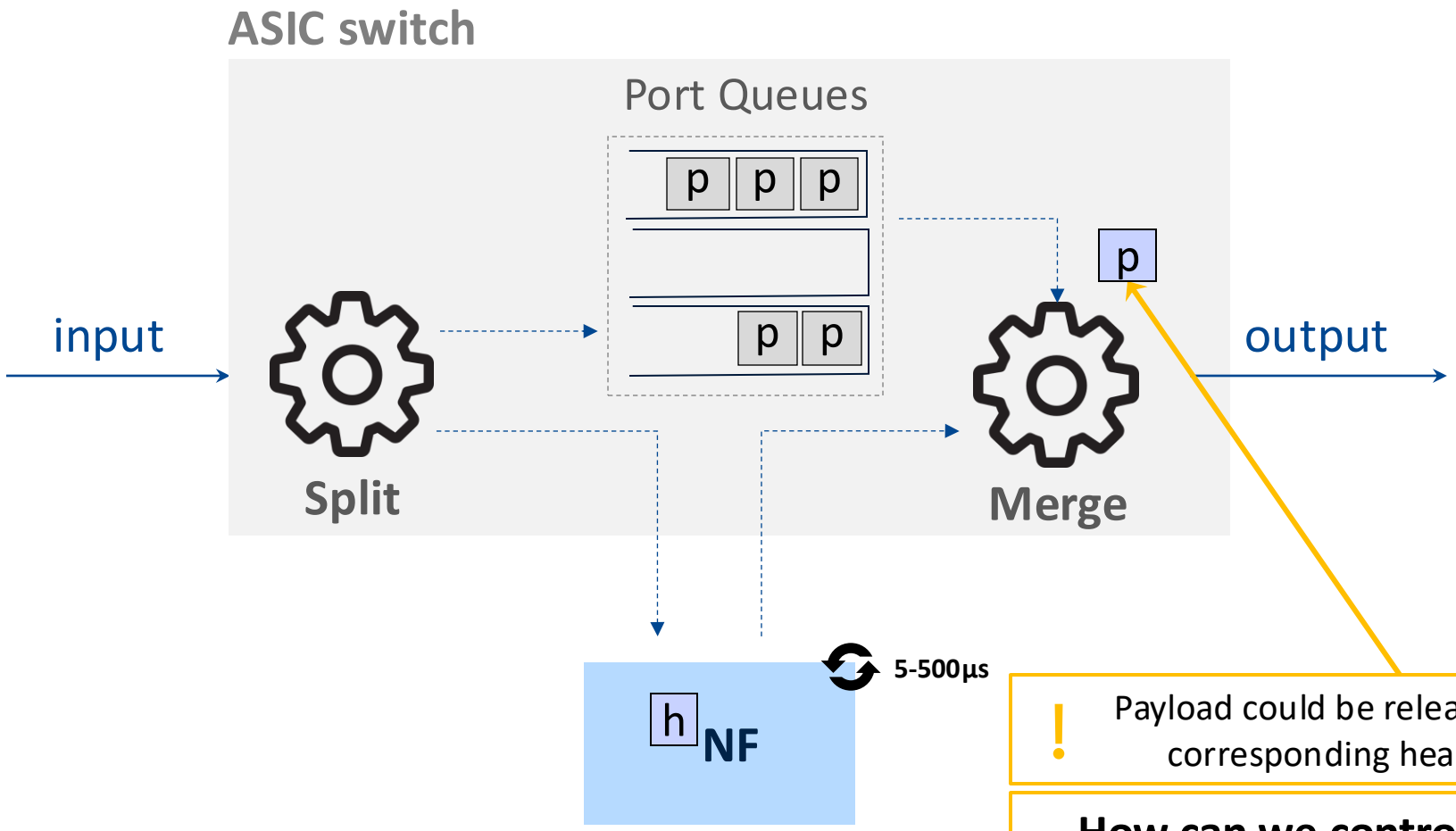
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Payload could be released before the corresponding header is back!
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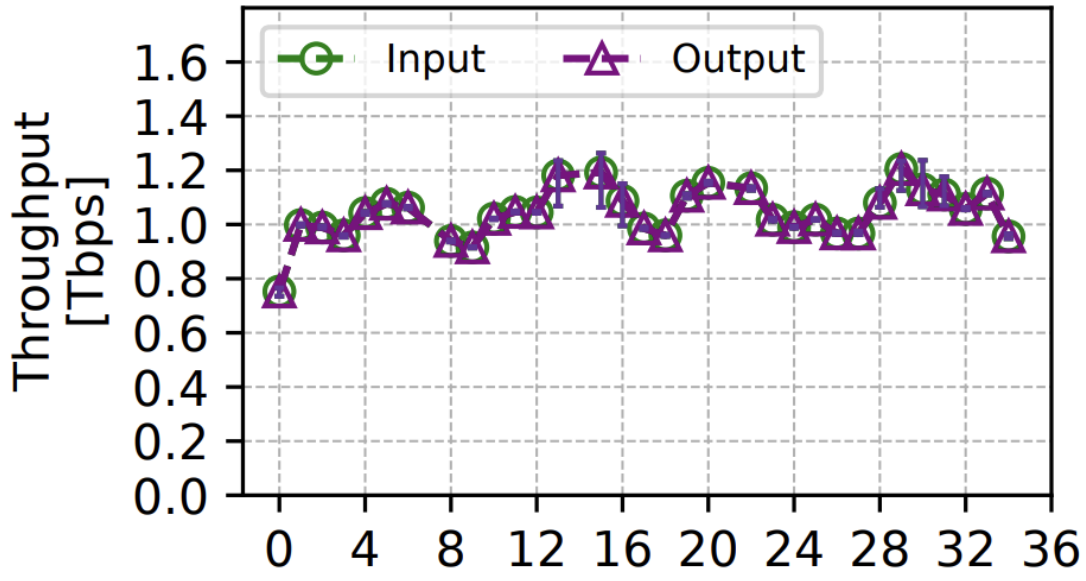
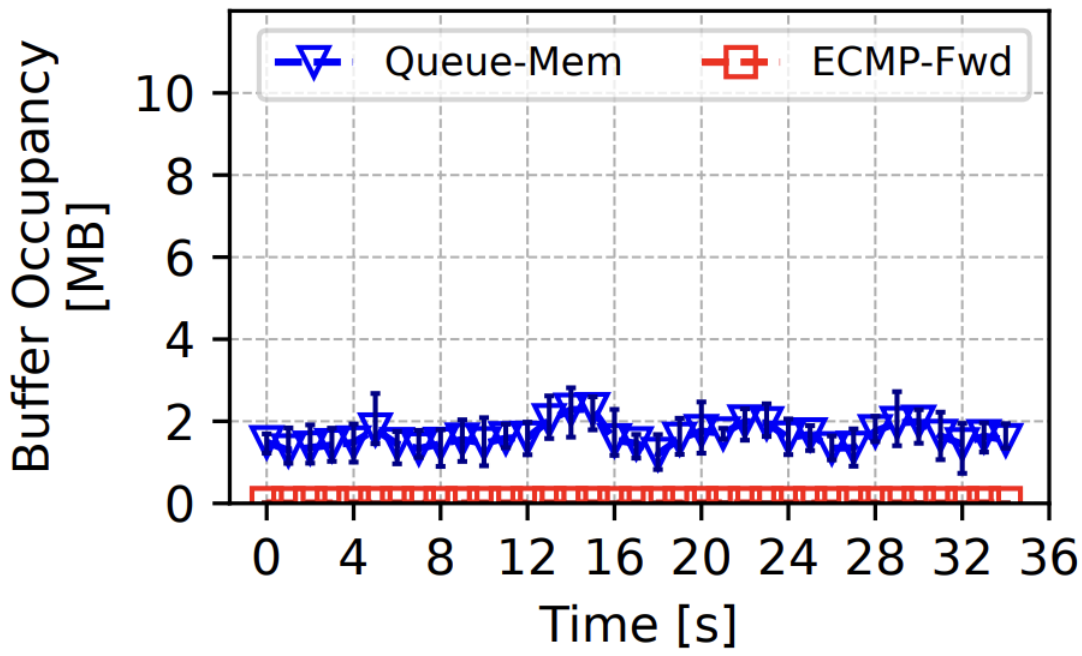
QueueMem

Stop the queue with Priority-Flow-Control (PFC)

Evalution of QueueMem (combined with FAJITA)

Network function: Per-flow counter + Load balancer + Per-flow rate limiter





FAJITA + QueueMem conclusions

The **FAJITA** system:

- **incorporates** the three essential principles for stateful packet processing **together**
- **minimizes** memory access overheads by **exploiting batching** & **software prefetching**
- **alleviates** overheads of accessing shared data structures **by introducing auxiliary HTs**
- achieves **performance 2x higher** than existing stateful packet processors
- demonstrates that dynamic inter-core load balancing is **detrimental** at high rates
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The **QueueMem** system (under submission):

- supports packet splitting entirely on the switch
- reduces power consumption
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