

State-Compute Replication: Parallelizing High-Speed Stateful Packet Processing

Academic Salon on High-Performance Ethernet: Host Networking and Monitoring

12 - 13 March 2025







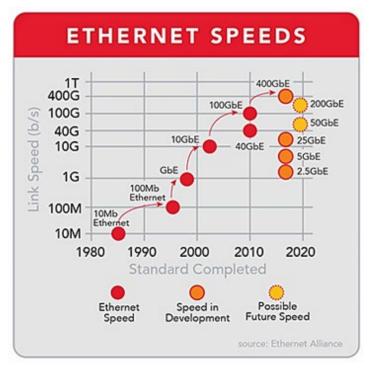
Software Packet Processing in post Moore's Law Era

- Throughput is a **first-class citizen** in modern networked systems
 - Software LBs, CDN nodes, DDoS mitigators depends on it

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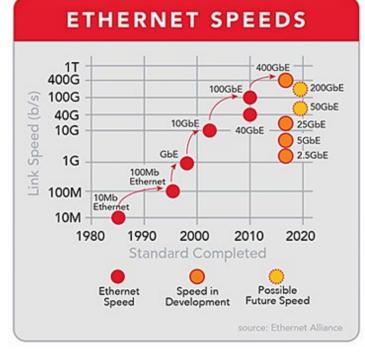
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Increasing NICs speed



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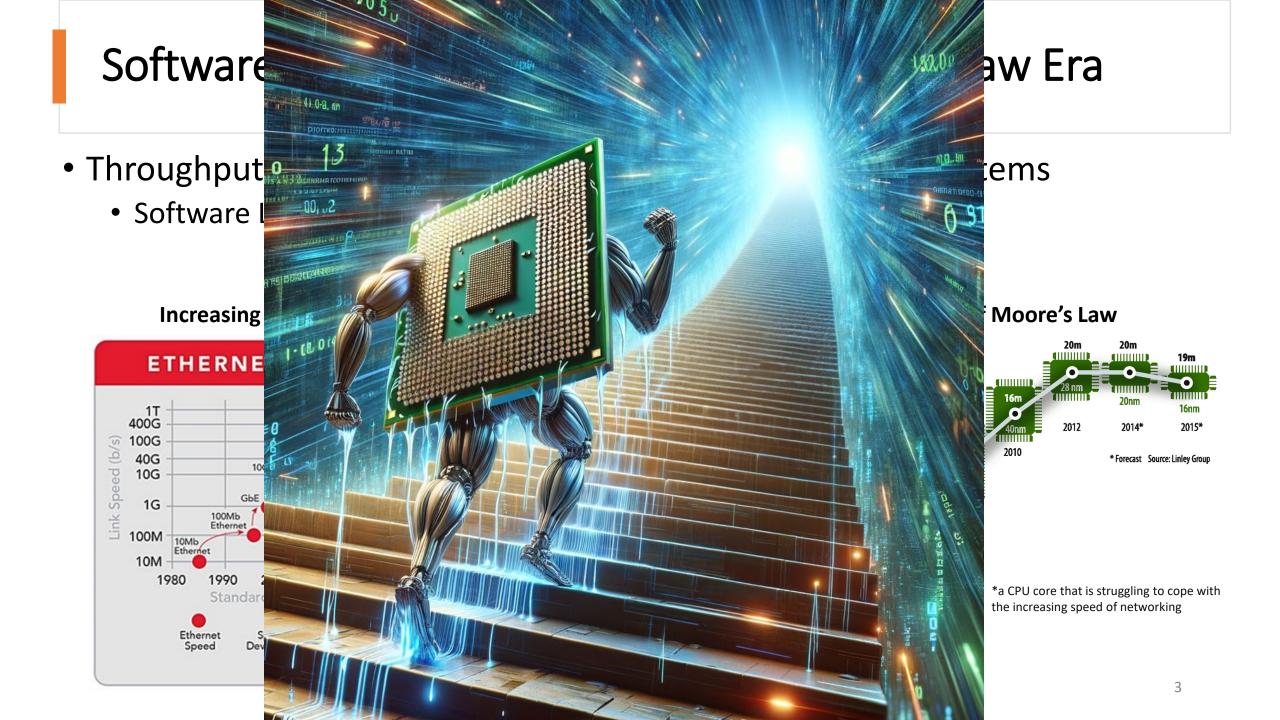
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Shrinking chips Number and length of transistors bought per \$ 16nm 2012 2015* 2014* * Forecast Source: Linley Group 2.6n 2006 2004 Nanometres (nm) 2002 2

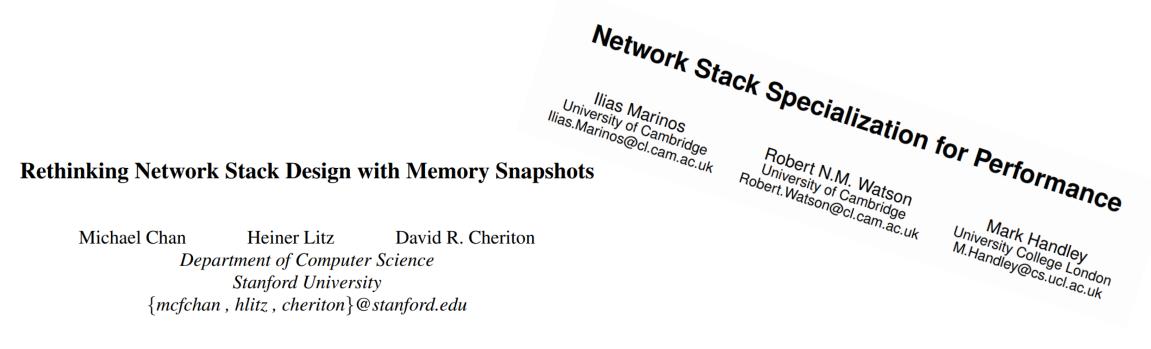
Increasing NICs speed

Slowdown of Moore's Law



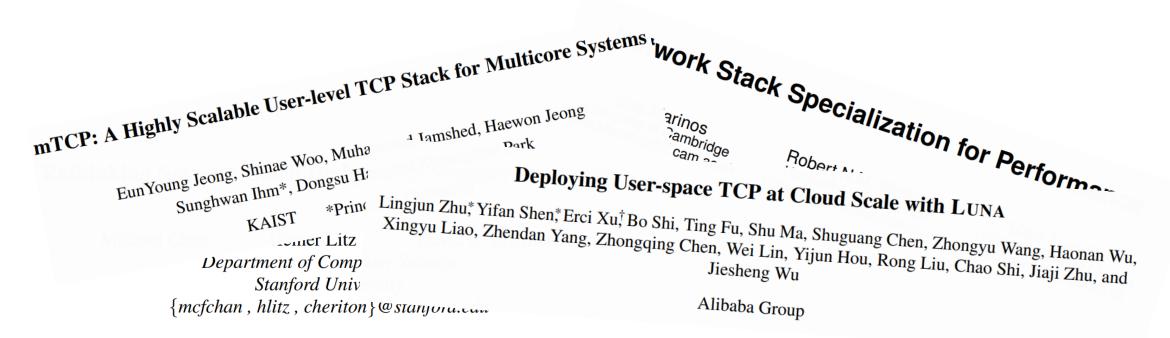
How to speed up packet processing?

- There have been significant efforts to speed up packet processing through
 - Better stack design



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 - Running software at lower layers of the stack



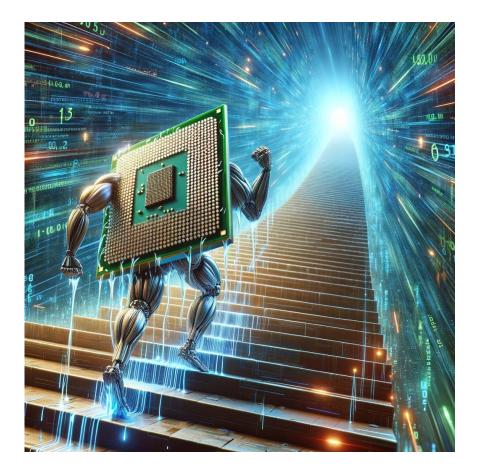
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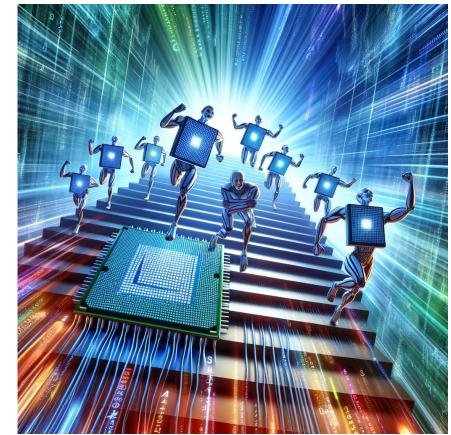
- There have been significant efforts to speed up packet processing through
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 - Removing user-kernel crossings
 - Running software at lower layers of the stack
 - Design better host interconnects

InoPLI. D. Jable Iptables k Stack o mTCP: A Highly Sci The nanoPU: Redesigning the CPU-Network Interface for Performan to Minimize RPC Tail Latency Securing Linu Stephen Ibanez, Alex Mallery, Serhat Arslan, Theo Jepsen, Sebastiano Miano LUNA Politecnico di Torino, Italy Muhammad Shahbaz, Nick McKeown, Changhoon Kim sebastiano.miano@polito.it ongyu Wang, Haonan Wu, Chao Shi, Jiaji Zhu, and Mauricio Vásquez Berna Stanford University Politecnico di Torino, Italy mauricio.vasquez@polito... Alloaba Group ., nultz, cheriton & @stanjoru.cum

This talk: Scaling Packet Processing using multiple cores

• We present a principle that enables scaling a single, stateful packet processing programs across multiple cores

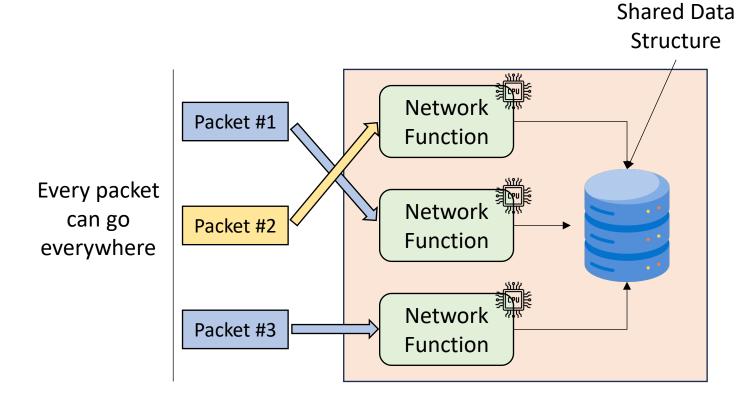




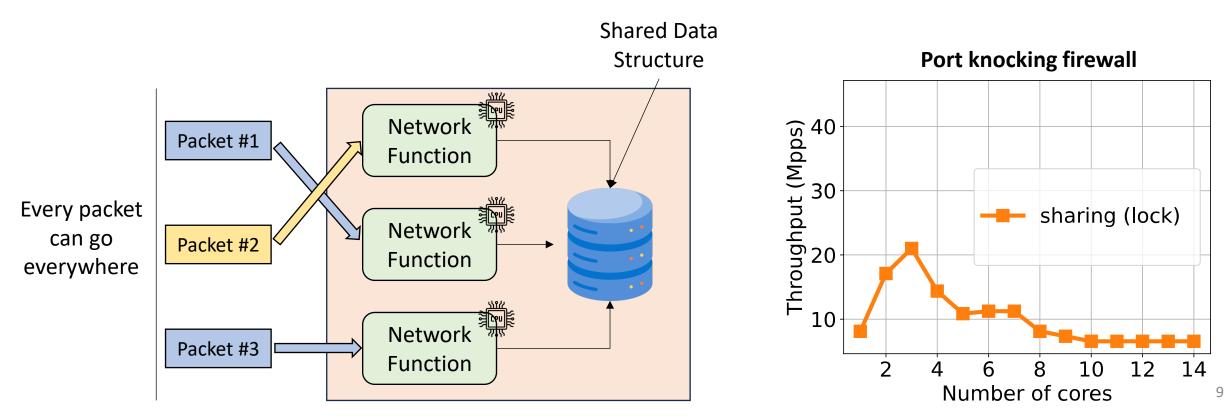
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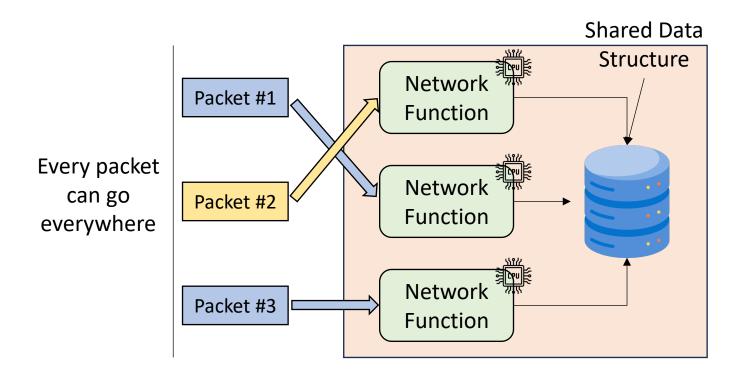
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- ...many packet processing applications are stateful
 - Maintain and update the regions of memory across many packets

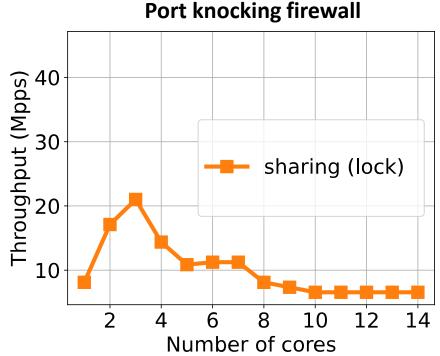
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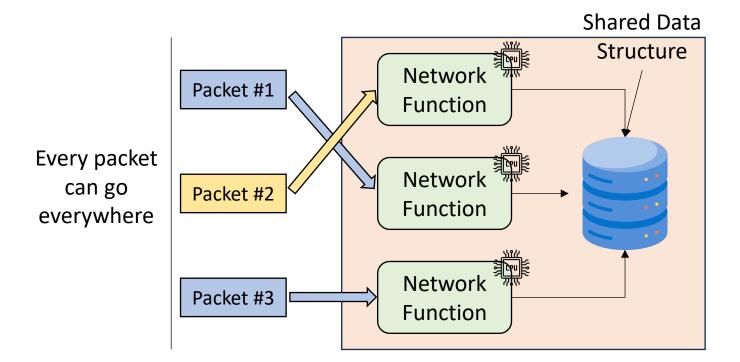






Flows in realistic network traffic follow heavy-tailed distributions

• Significant memory contention if packet are spread across cores



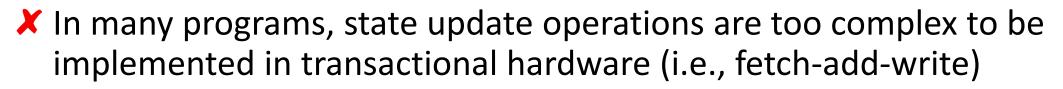
(sd 40 30 30 10 2 4 6 8 10 12 14 Number of cores

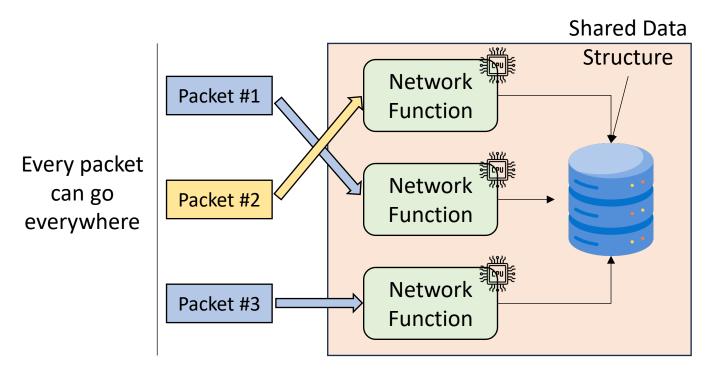


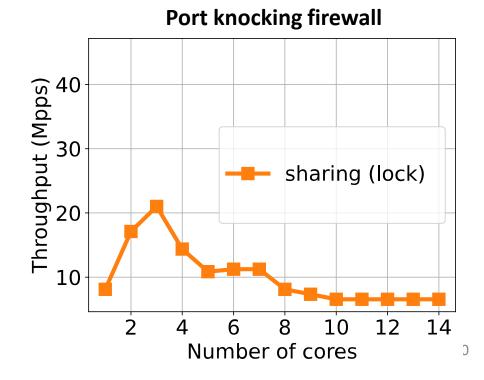


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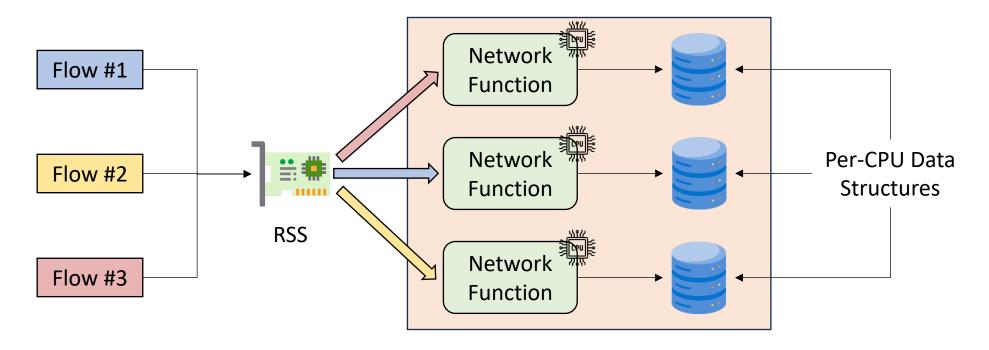


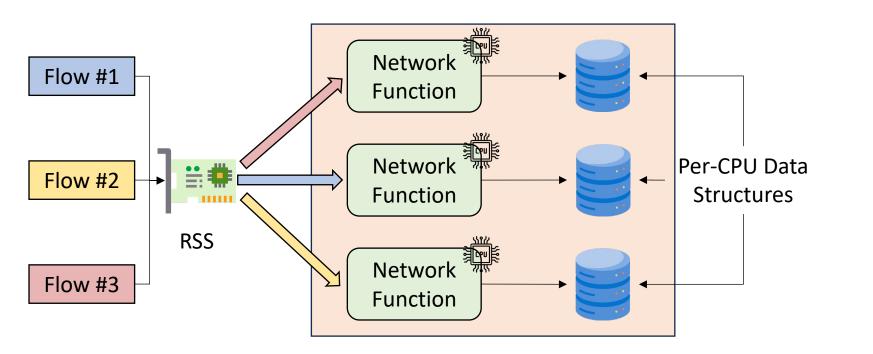




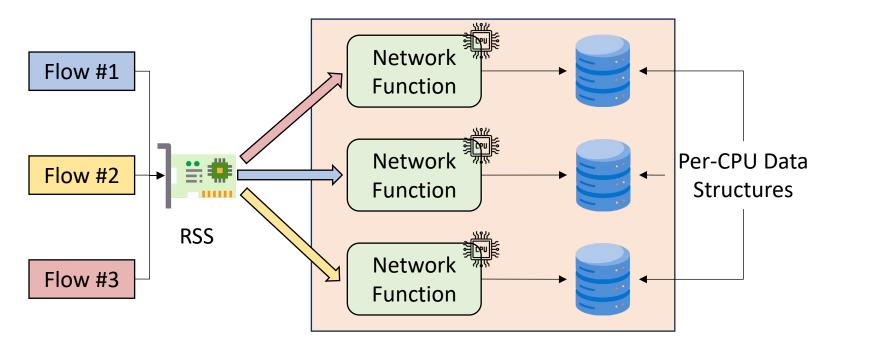
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 - NIC RSS to direct packets from the same flow to the same core + shared-nothing data structures
 - The most used technique today

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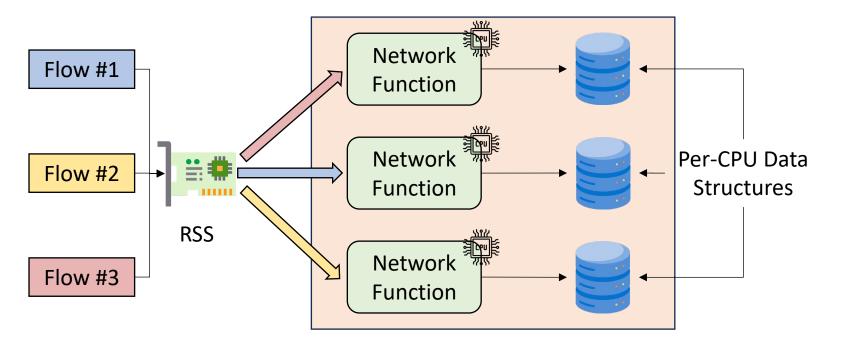




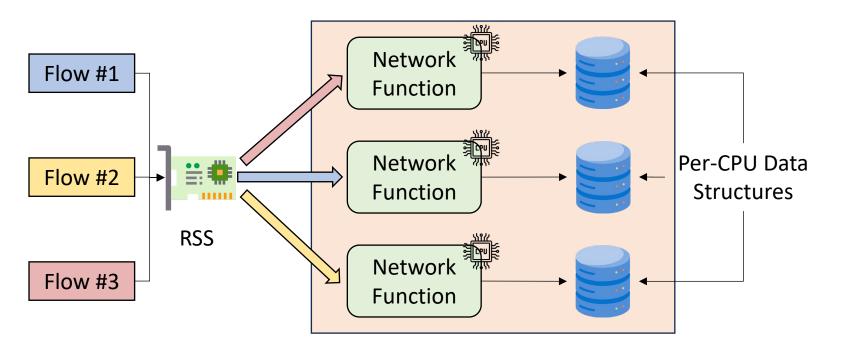
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 - There may be parts of the program state shared across packets (e.g., list of free ports in a NAT)



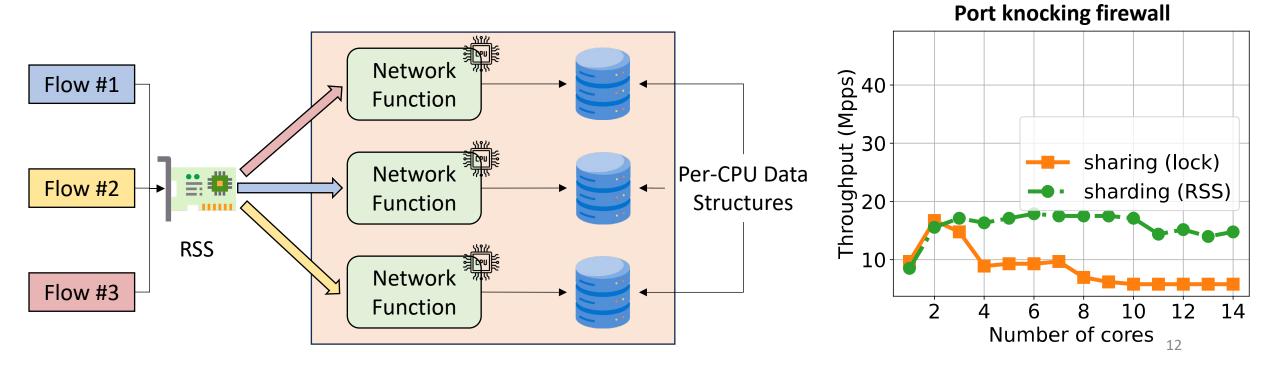
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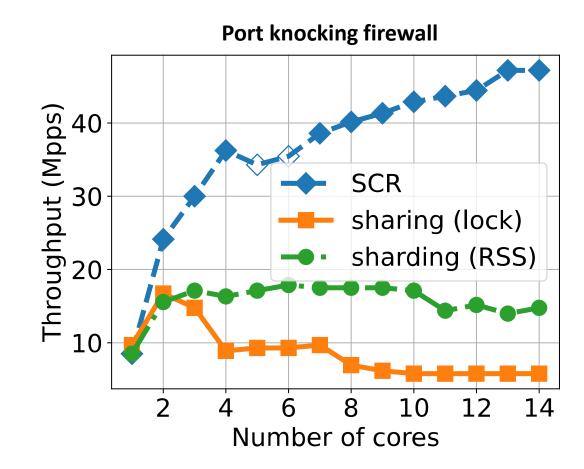


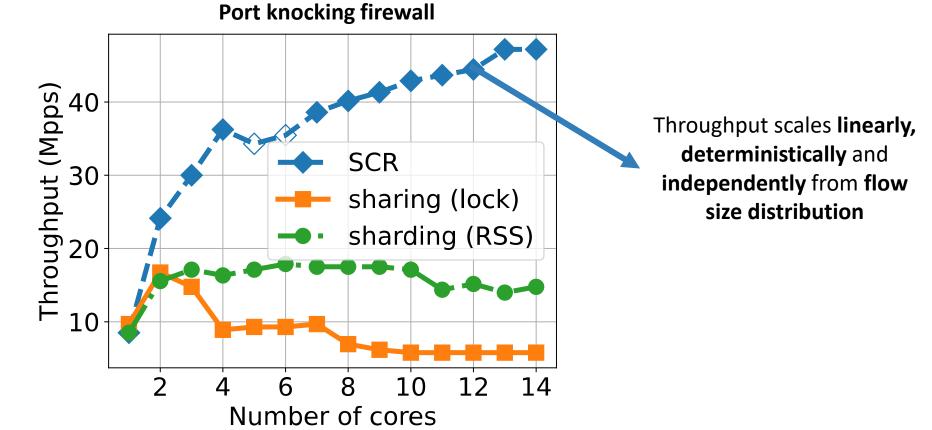
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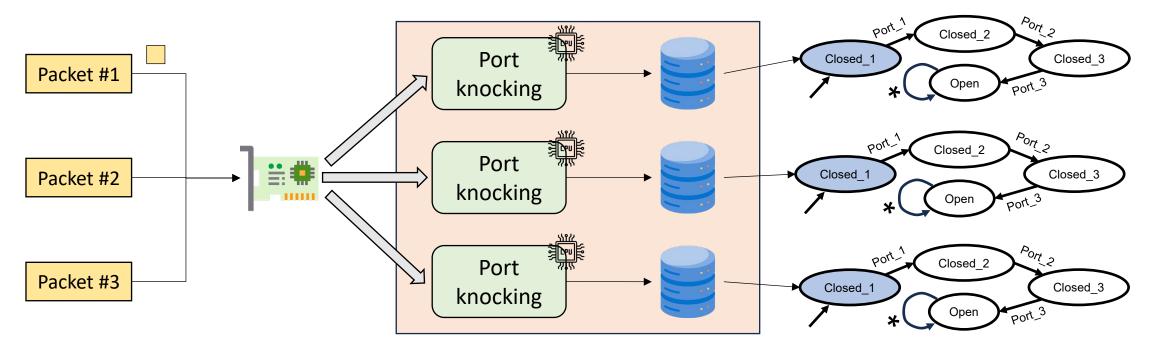




How does this work? – Running Example

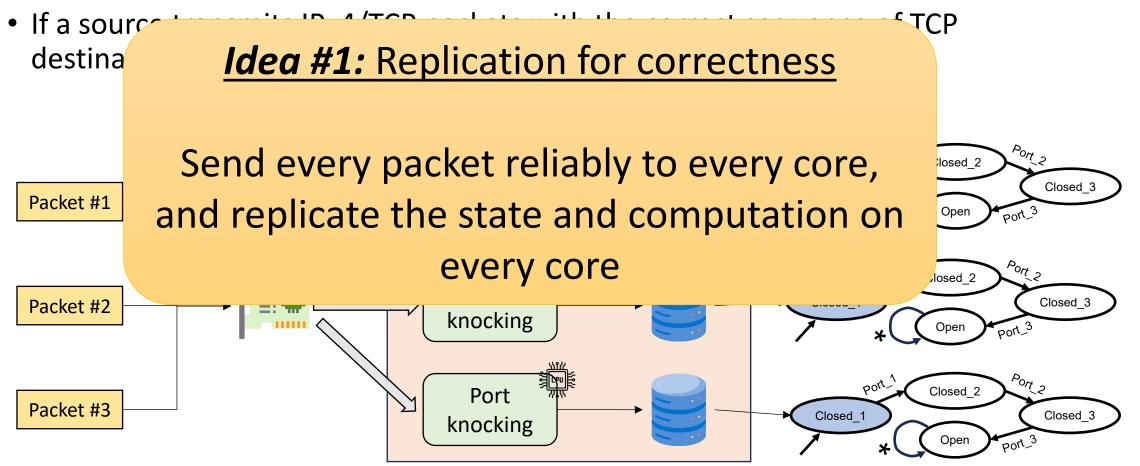
• Port knocking firewall

• If a source transmits IPv4/TCP packets with the correct sequence of TCP destination ports, all further communication is permitted



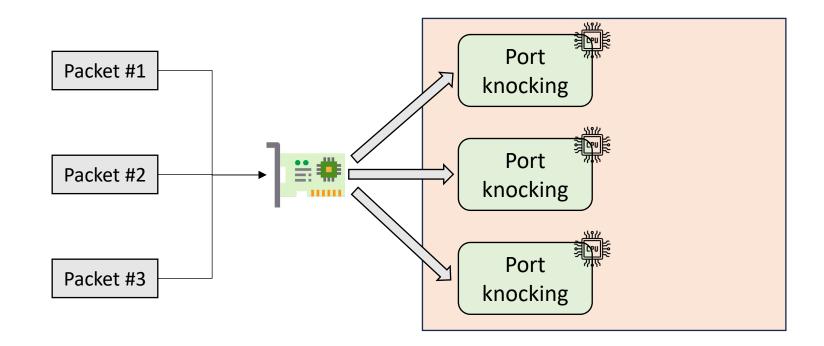
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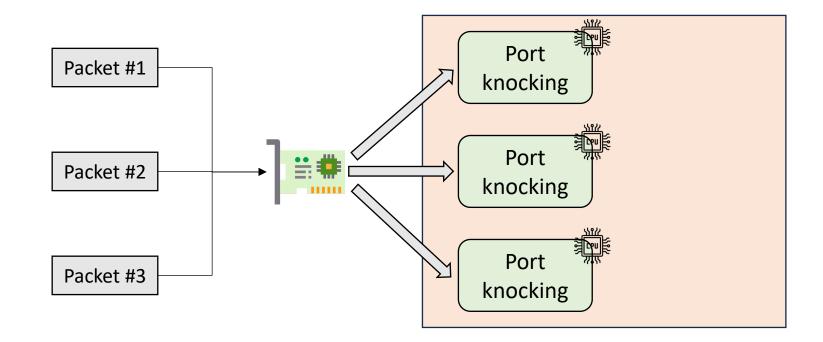


• Packets can be perfectly sprayed across all the cores (or a set of cores)

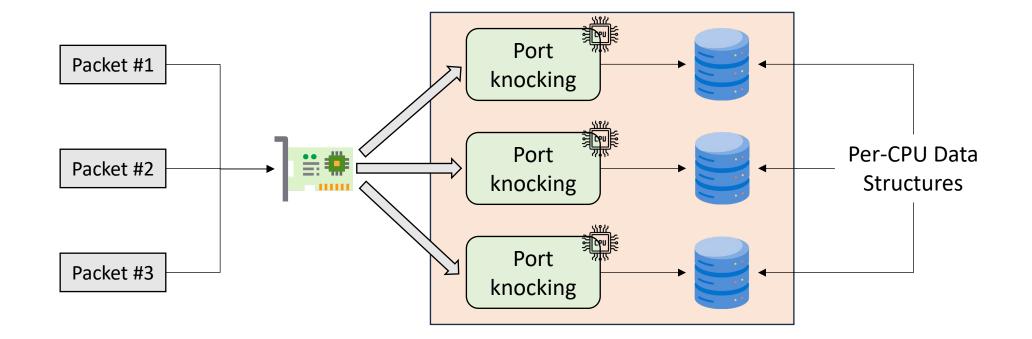
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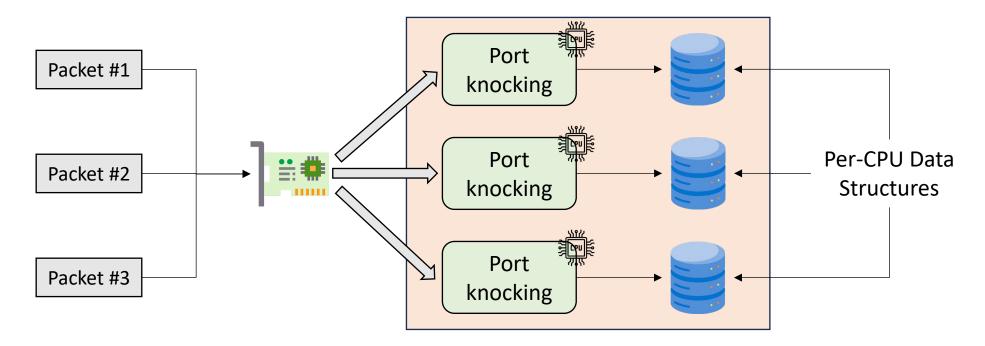
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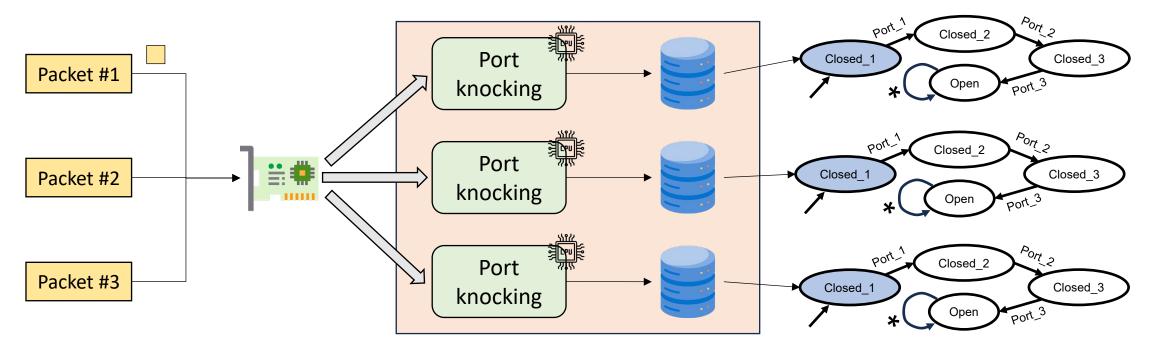
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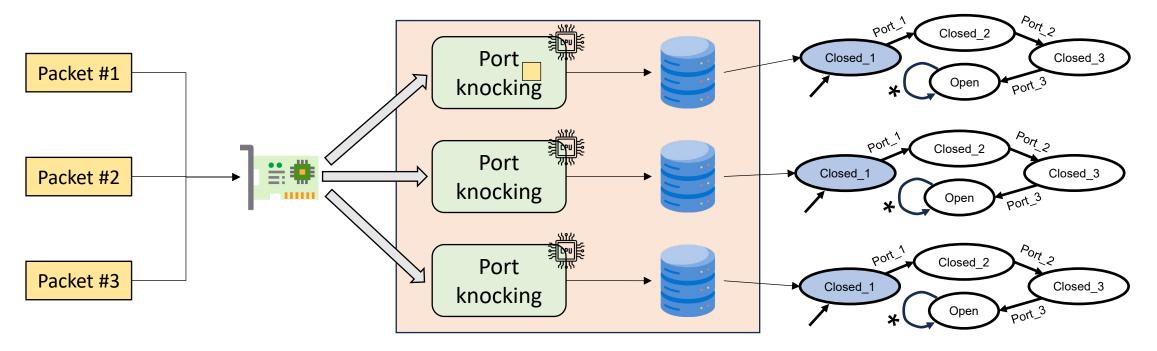
- Packets can be perfectly sprayed across all the cores (or a set of cores)
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- Given a set of N cores, every packet p will go to core c = p % (N − 1)



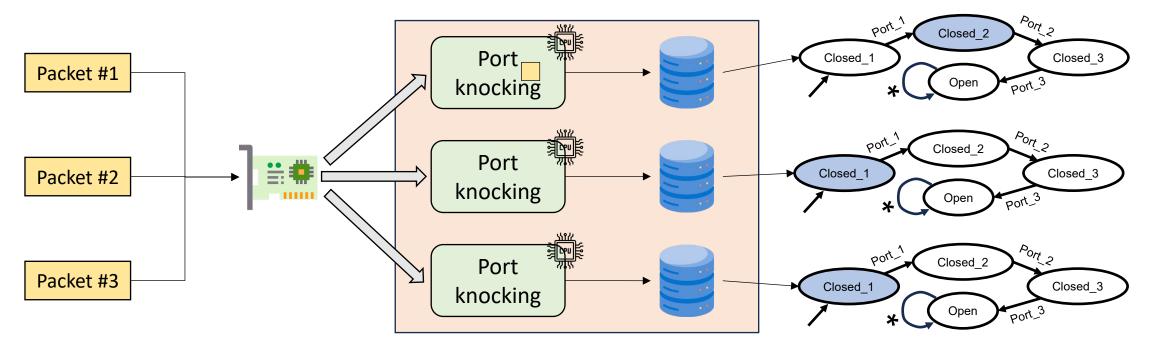
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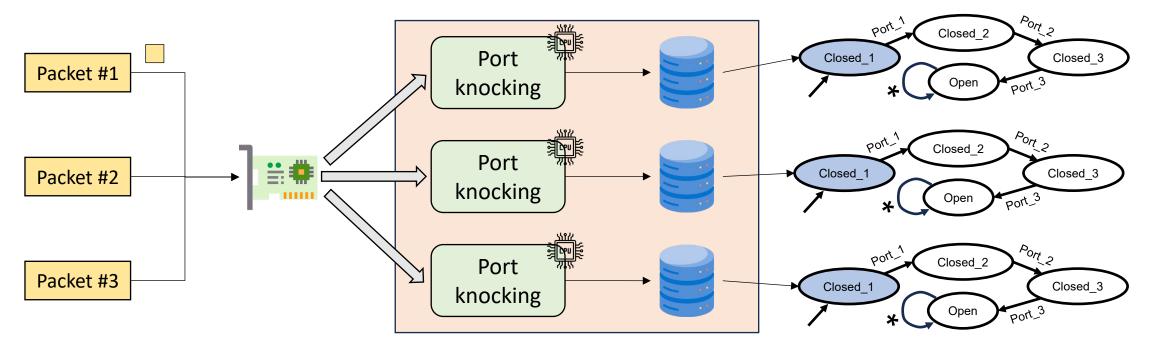
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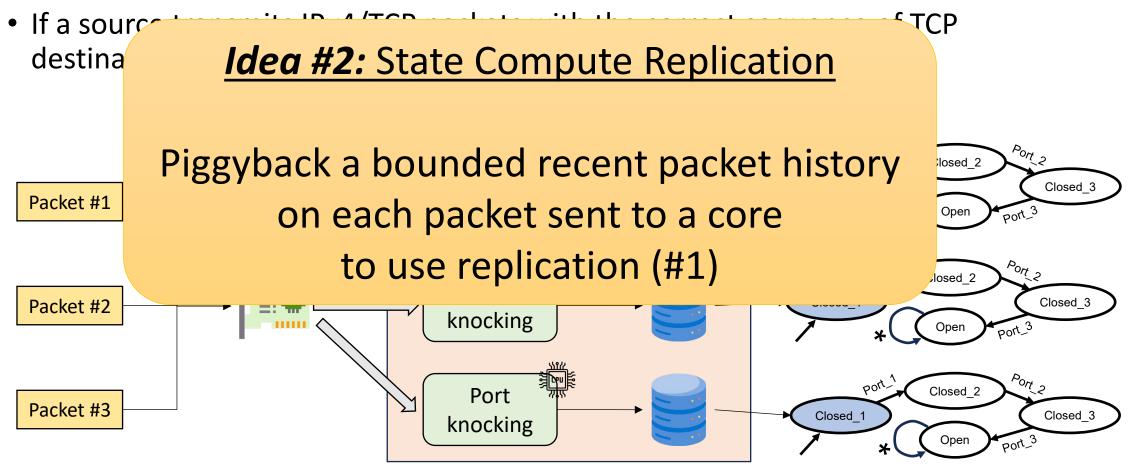
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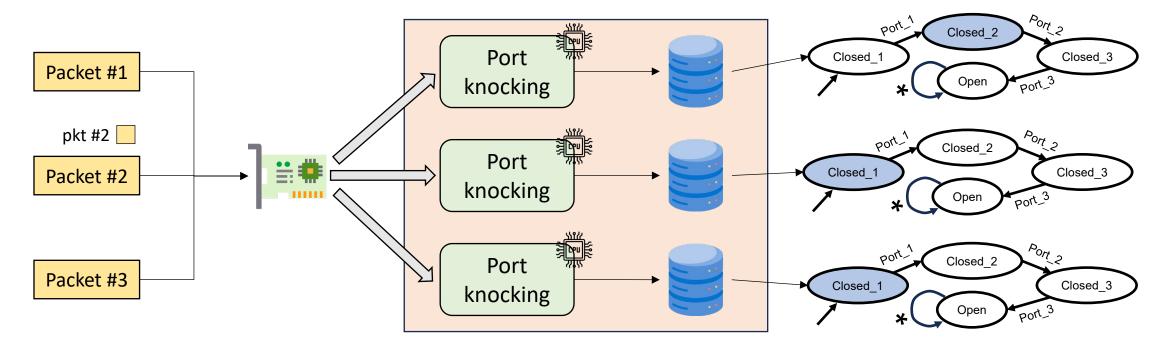


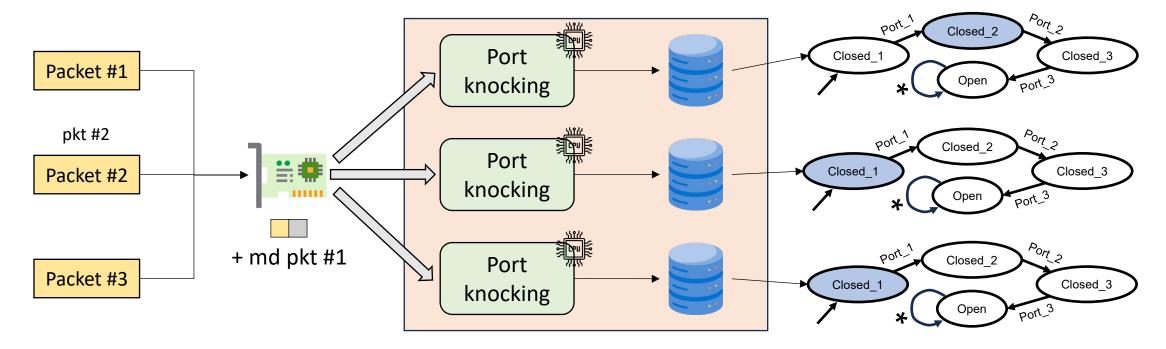
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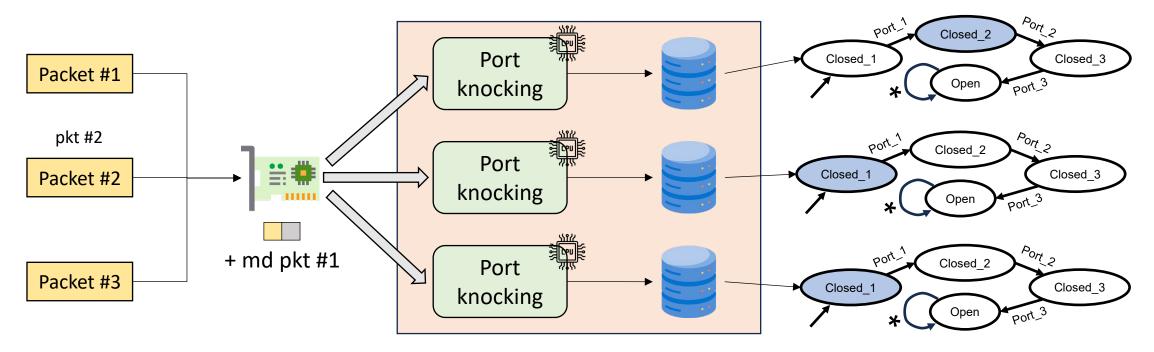
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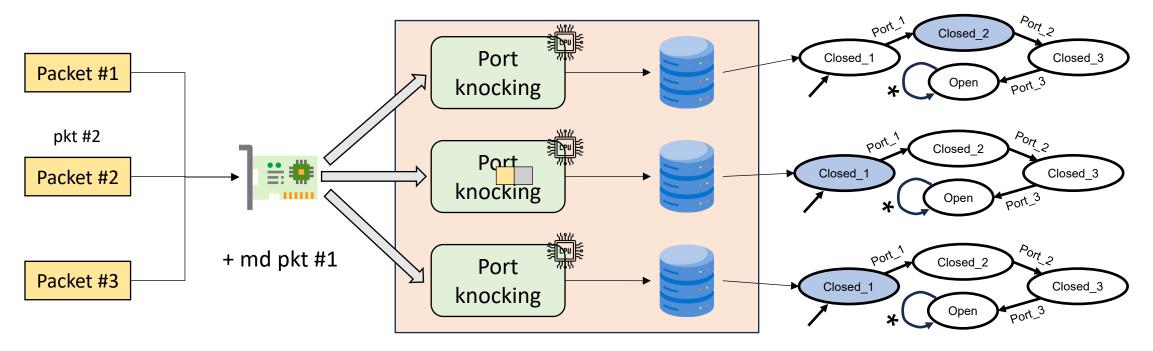




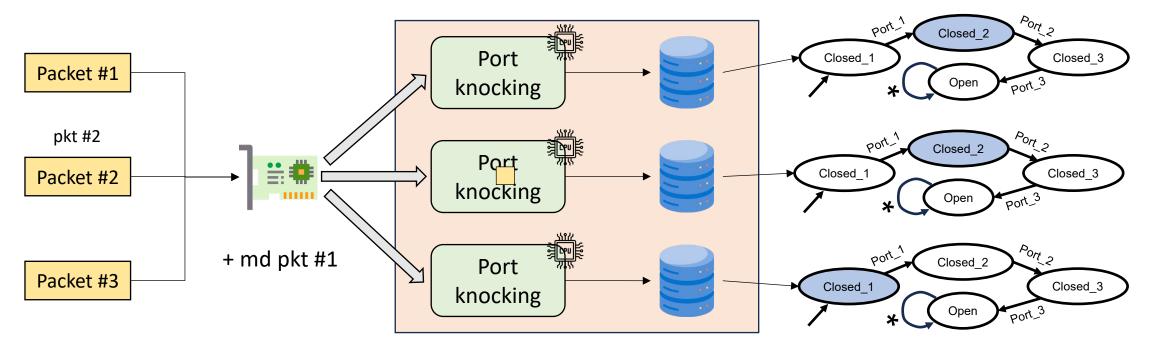
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 - In this example: I3proto, I4proto, srcIP, dstPort



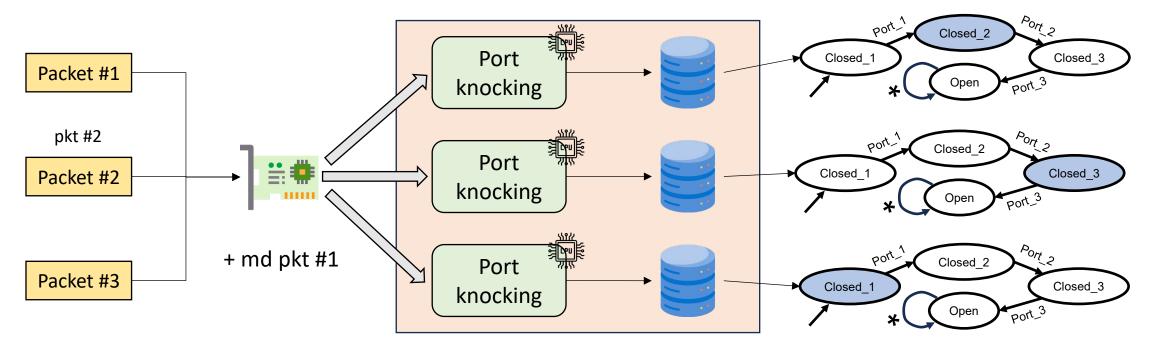
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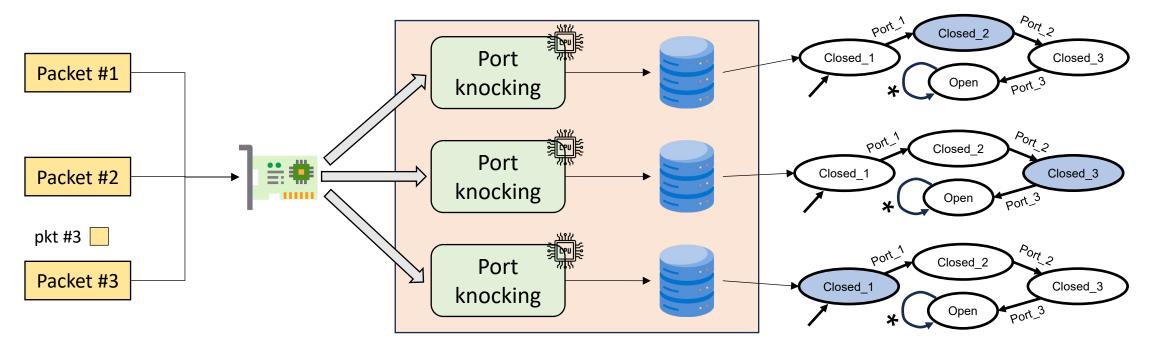
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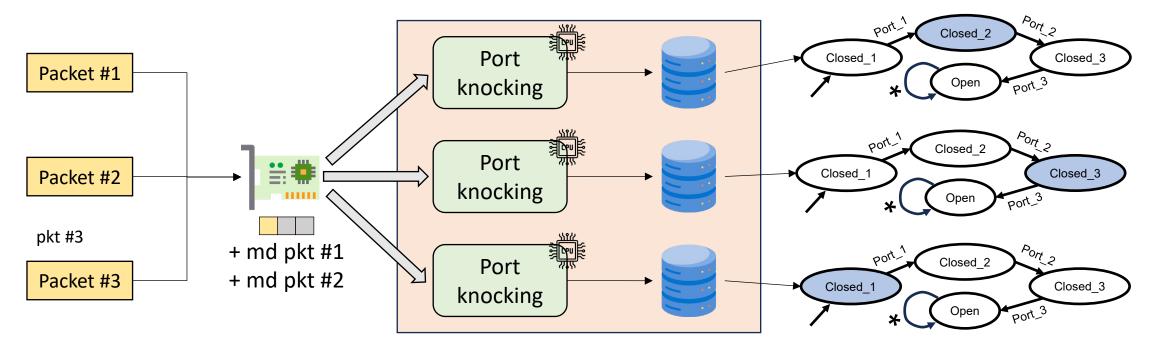
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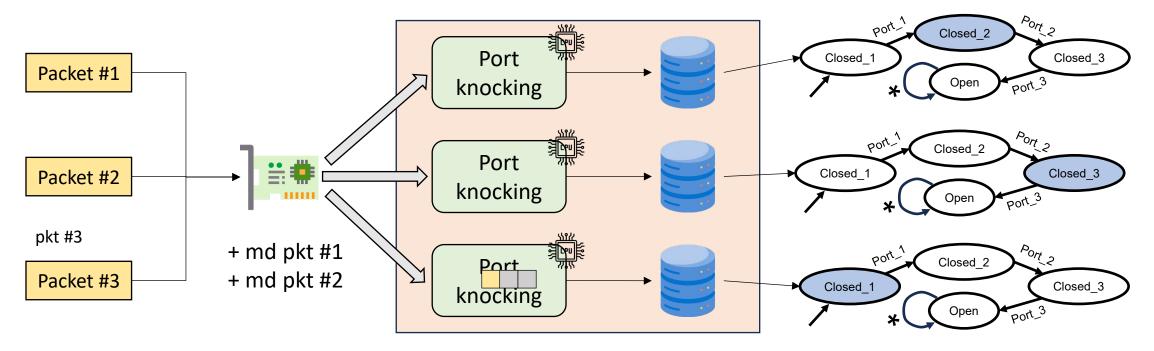
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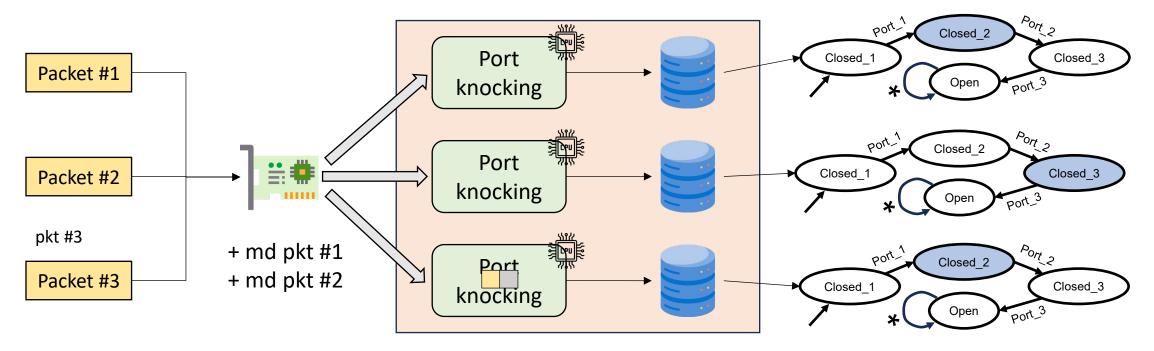
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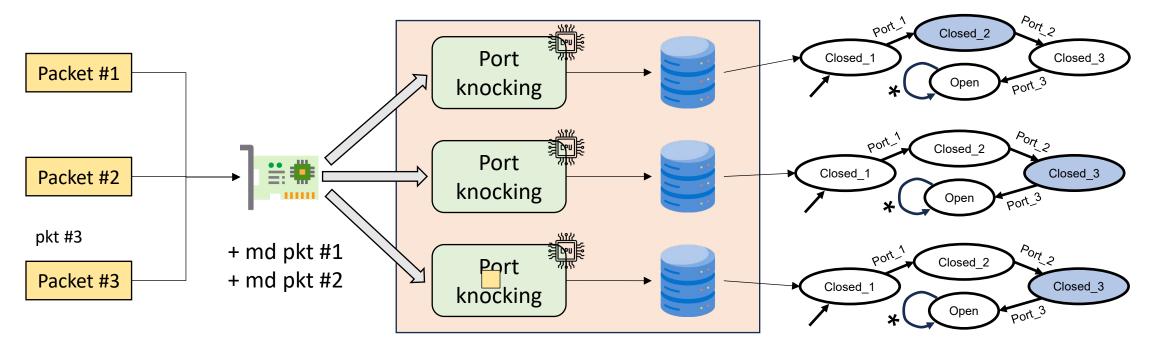
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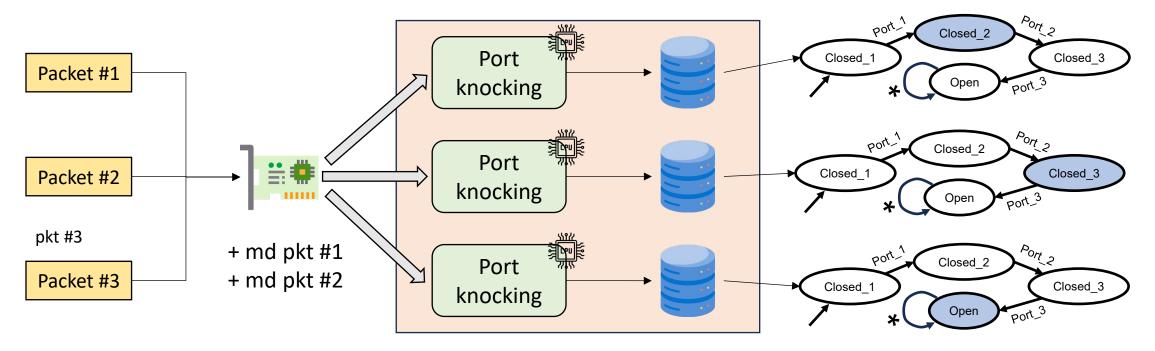
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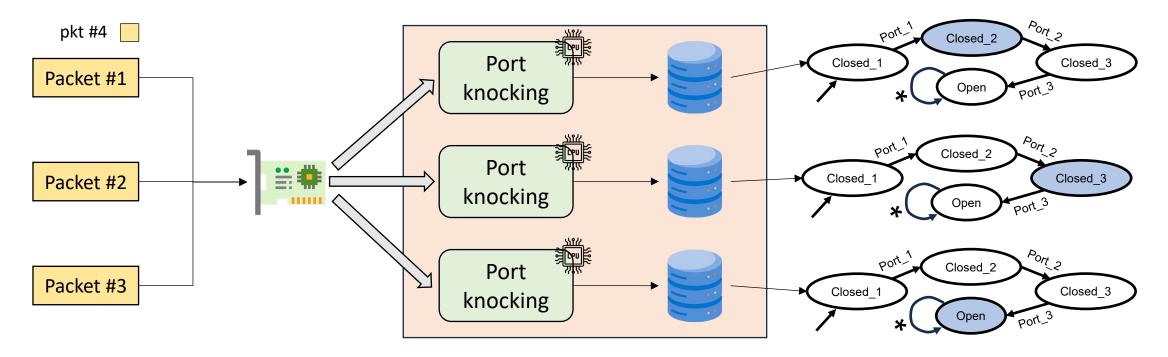


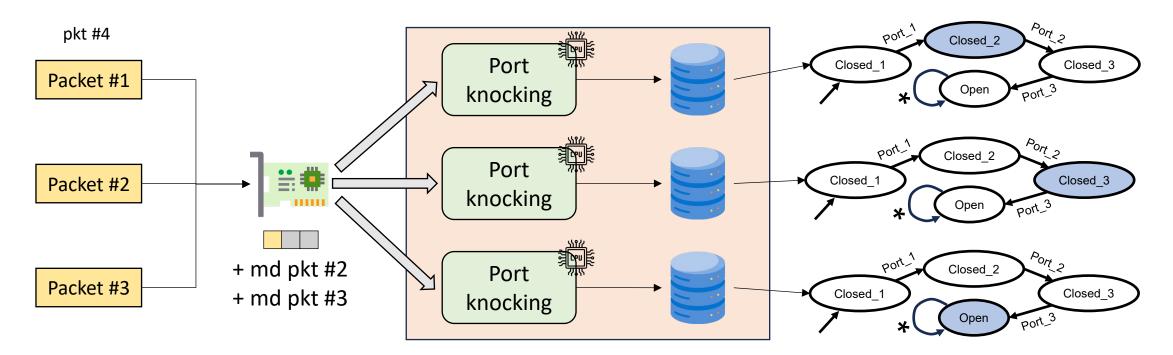
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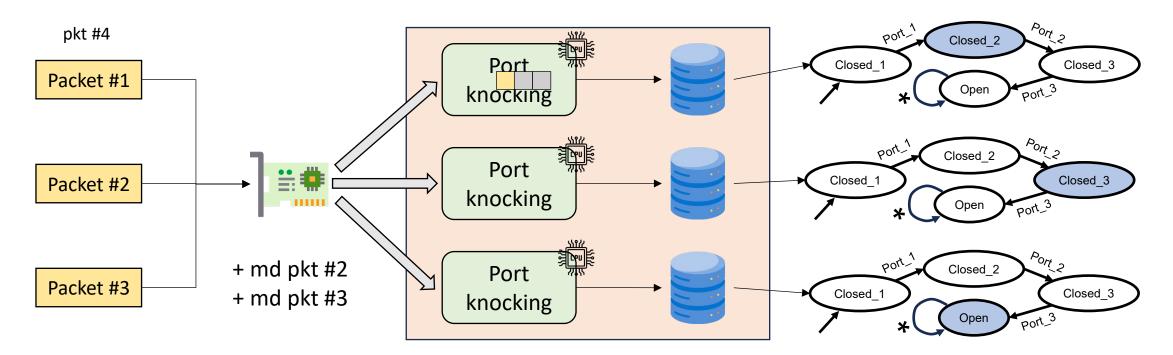


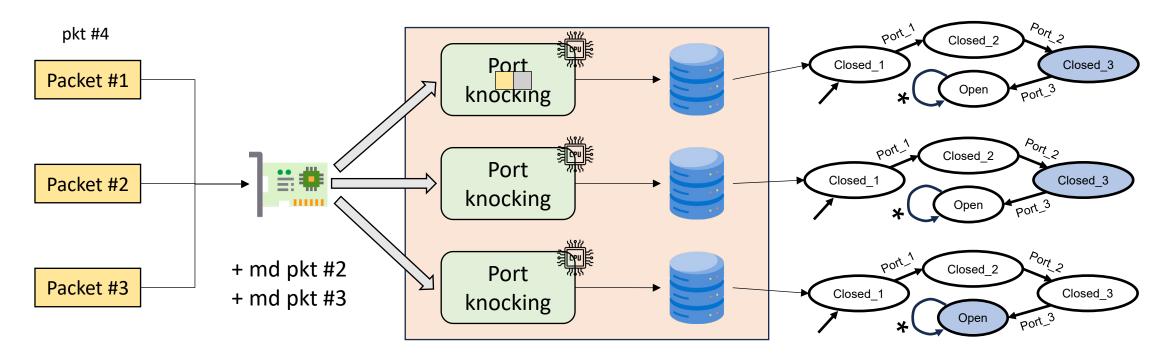
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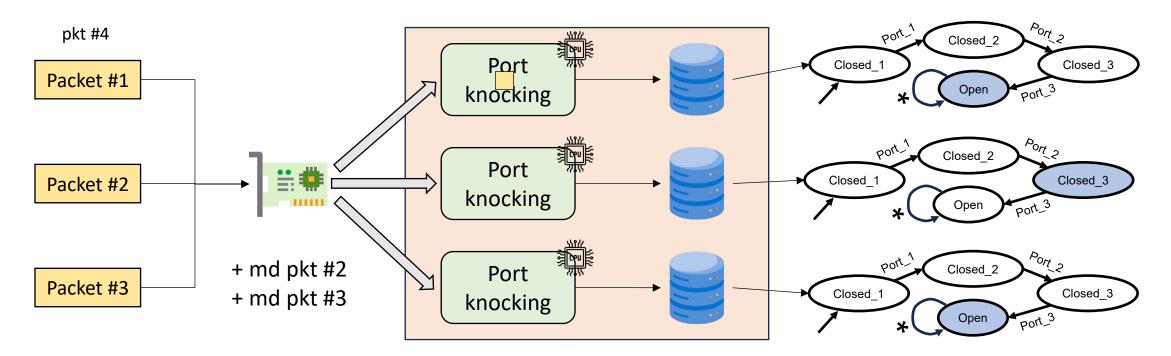




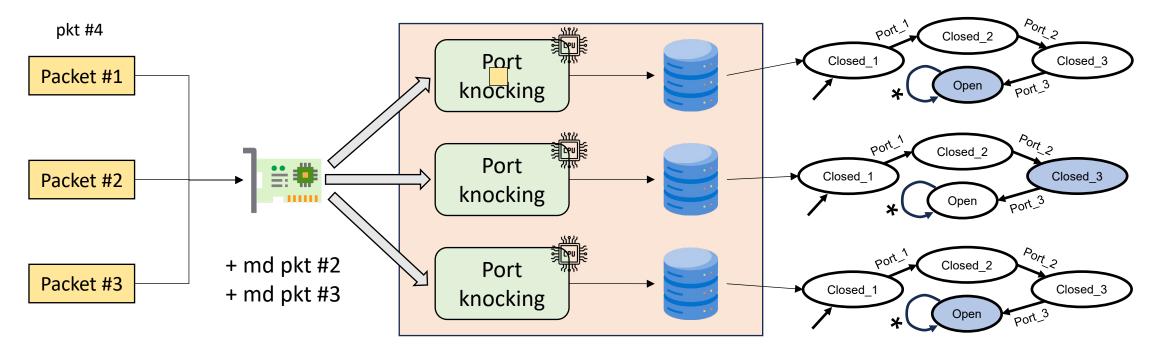


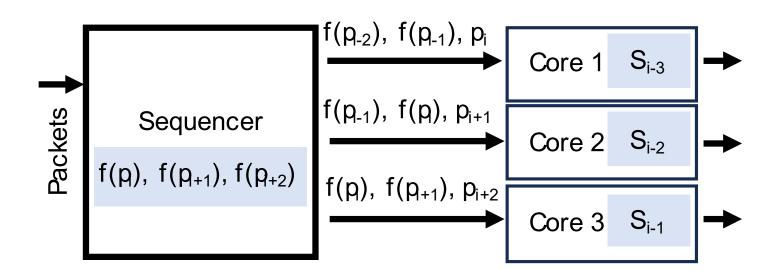




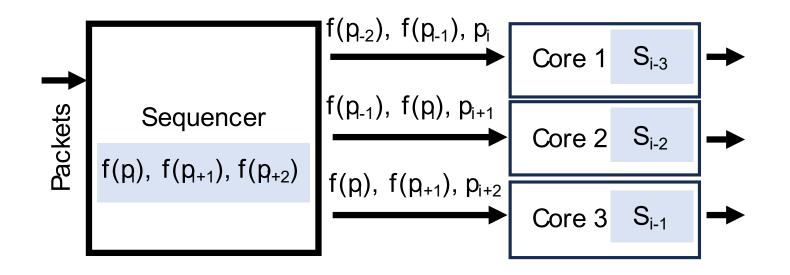


- In general, every packet has:
 - Current pkt + $\sum md(N-1)$
 - Where N is the number of cores

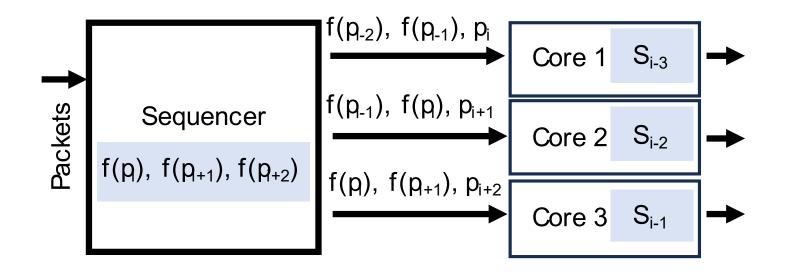




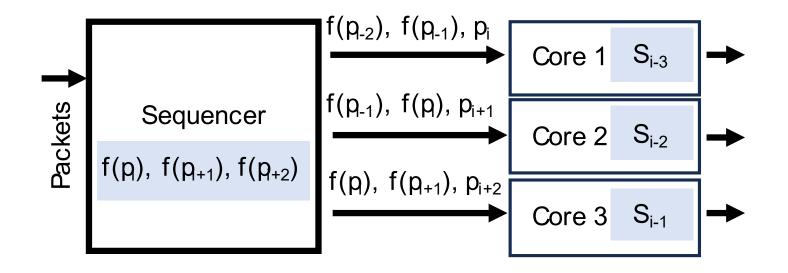
1. Steer packets across cores in round-robin fashion



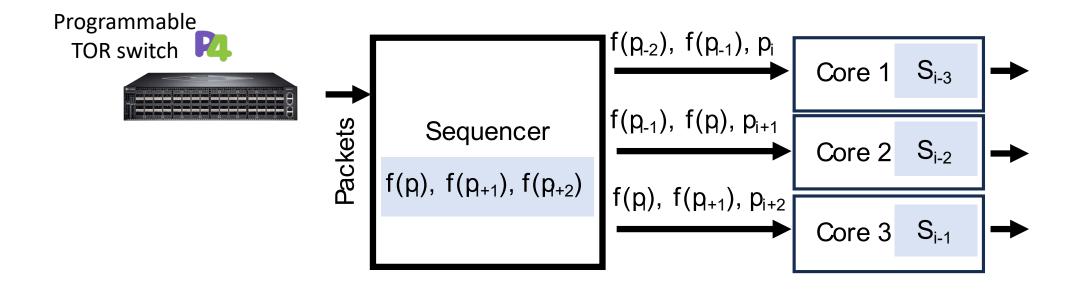
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- 2. Maintain the most recent packet history across all packets



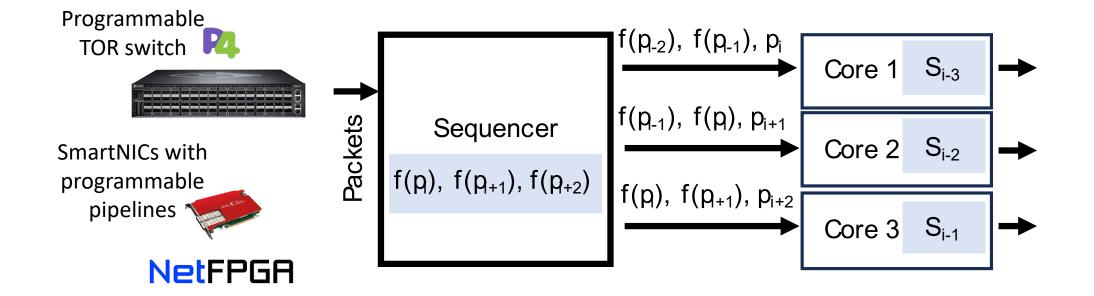
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Operationalizing SCR: SCR-Aware Programming

•••

+ sizeof(index);

```
int l3proto, l4proto, srcip, dport, i, j;
for (j = 0; j < NUM_META; j++) {
  i = (index + j) % NUM_META; // ring buffer
  struct meta *pkt = data + i * sizeof(meta);
  l3proto = pkt->l3proto;
  l4proto = pkt->l4proto;
  srcip = pkt->srcip;
  dport = pkt->dport;
  if (l3proto != IPv4 || l4proto != TCP)
     continue; // no state txns or pkt verdicts
  /* Update state for this srcip and dport: */
  /* map_lookup; get_new_state; map_update. */
  /* Note: No pkt verdicts for historic pkts.
}/
pkt_start = data +
  NUM_META * sizeof(struct meta)
```

•••

struct ethhdr* eth = pkt_start; // parse Ethernet
int l3proto = eth->proto; // layer-3 protocol
int off = sizeof(struct ethhdr);

struct iphdr* iph = pkt_start + off; int l4proto = iph->protocol; // layer-4 protocol if (l3proto != IPv4 || l4proto != TCP) return XDP_DROP; // drop non IPv4/TCP pkts

int srcip = iph->src; // source IP addr
off += sizeof(struct iphdr);
struct tcphdr* tcp = pkt_start + off;
int dport = tcp->dport; // TCP dst port

/* Extract & update firewall state for this src. *, int state = map_lookup(states, srcip); int new_state = get_new_state(state, dport); map_update(states, srcip, new_state);

/* Final packet verdict */
if (new_state == OPEN)
 return XDP_TX; // allow traversal

return XDP_DROP; // drop everything else

Operationalizing SCR: SCR-Aware Programming

• Define per-core state data structures and per-packet metadata structures.

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Operationalizing SCR: SCR-Aware Programming

- Define per-core state data structures and per-packet metadata structures.
- Fast-forward the state machine using the packet history.


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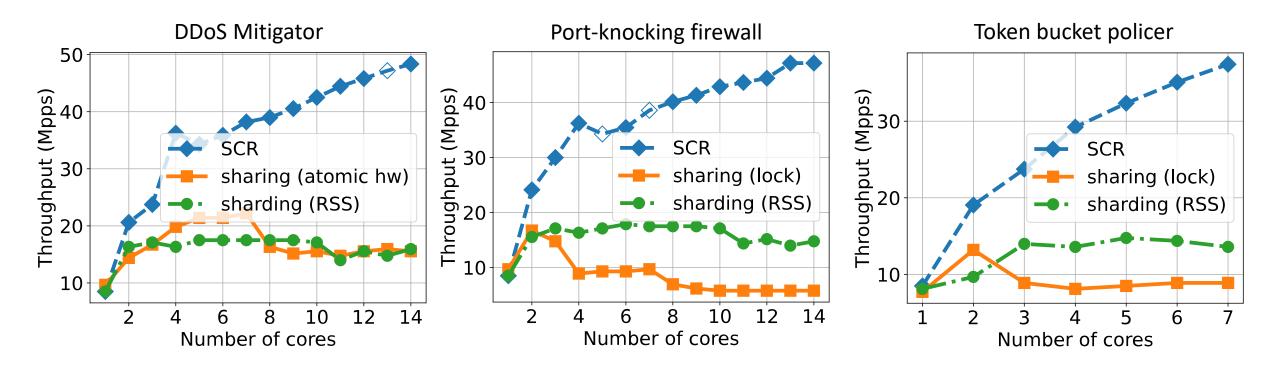
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Experimental Results - Throughput

• We tested SCR on a set of eBPF/XDP applications, using realistic traffic traces (CAIDA, University DC)



Experimental Results - Throughput

50

10

2

4

8

Number of cores

10

12

14

2

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• We tested SCR on a set of eRPE/XDP applications, using realistic traffic traces (C

SCR is the only scaling technique that can scale the throughput of all the stateful packet-processing programs we evaluated across multiple cores, regardless of the flow size distribution.

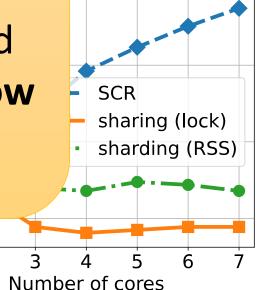
8

Number of cores

12

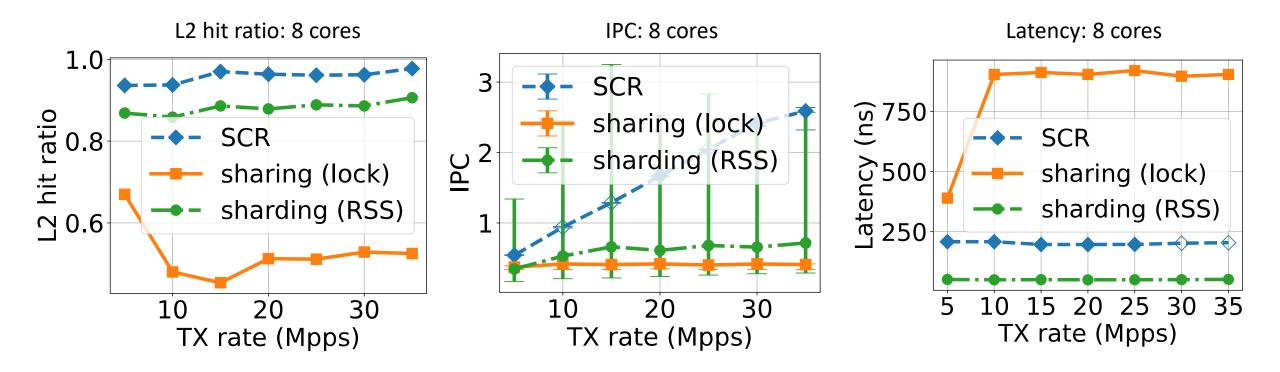
14



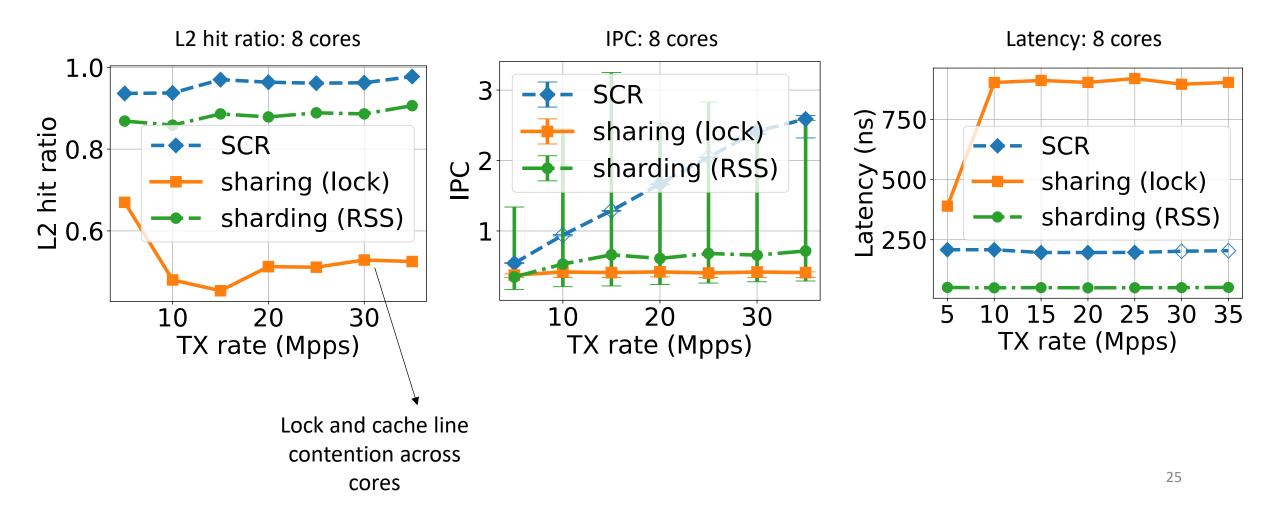


TO

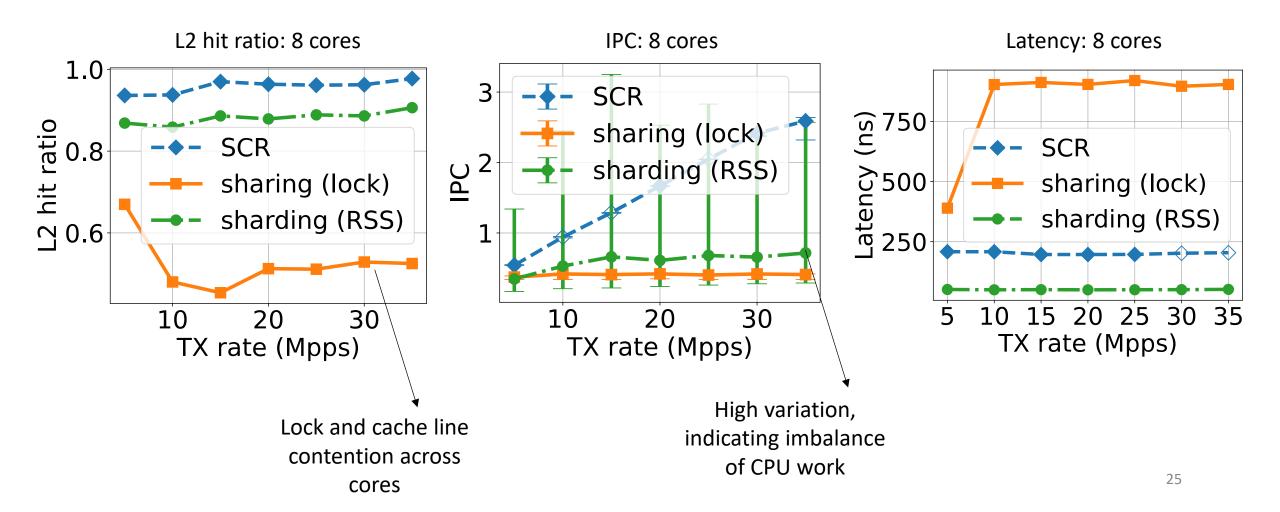
Why does SCR scales better than the other techniques?



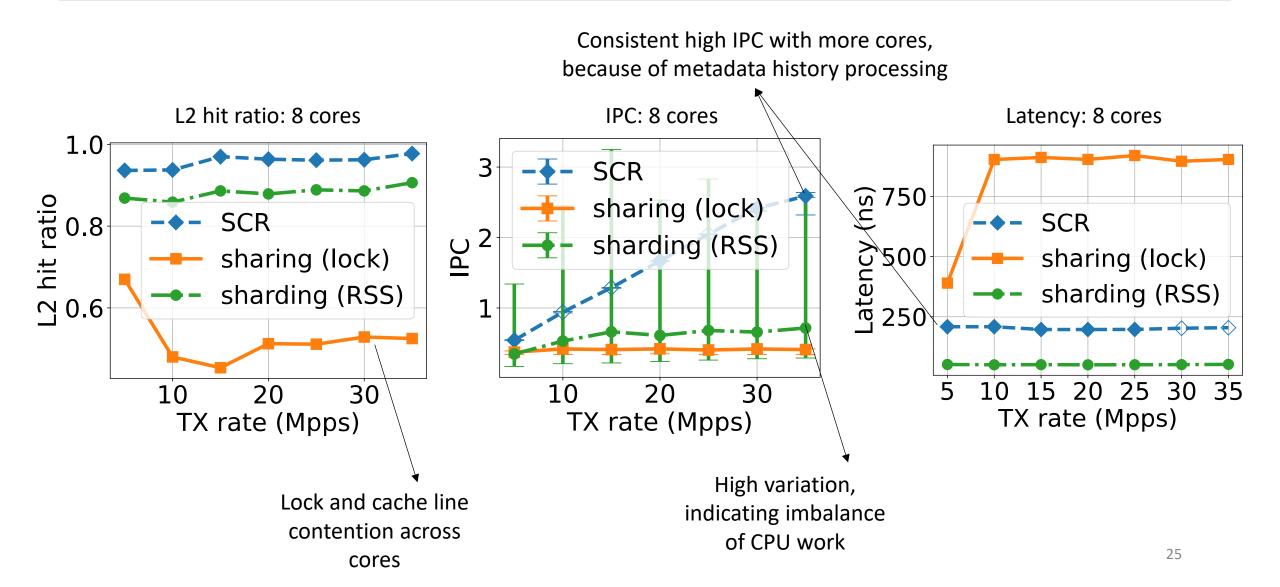
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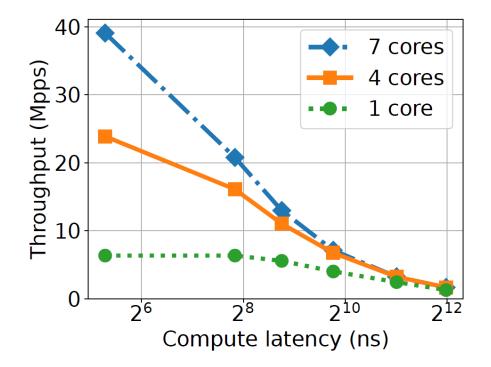
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Why does SCR scales better than the other techniques?



- 1. If the compute latency increases in comparison to the dispatch latency, the effectiveness of SCR's multi-core scaling reduces
 - Every core has to do "more work" to catch up with the state



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token bucket policer

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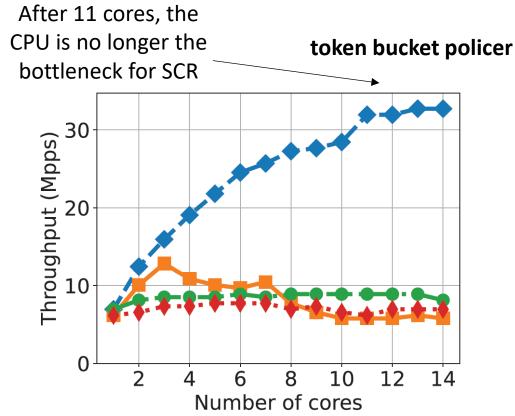
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- Increases PCIe transactions and bandwidth

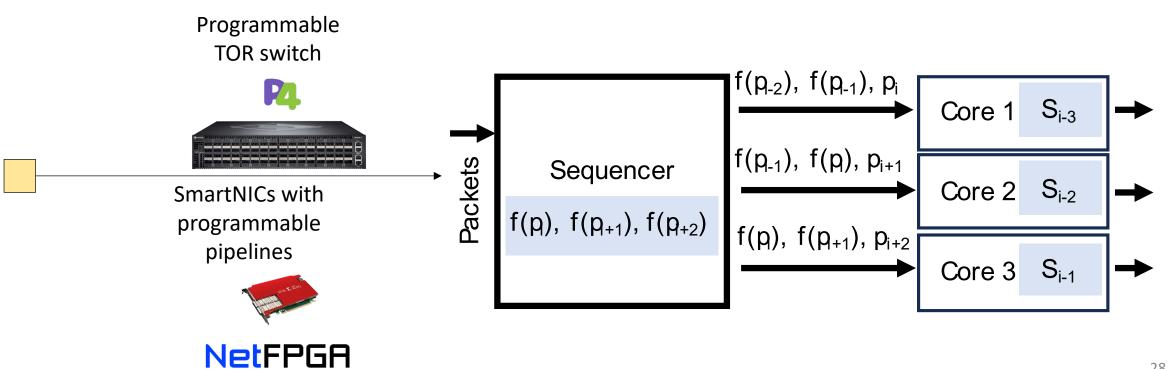
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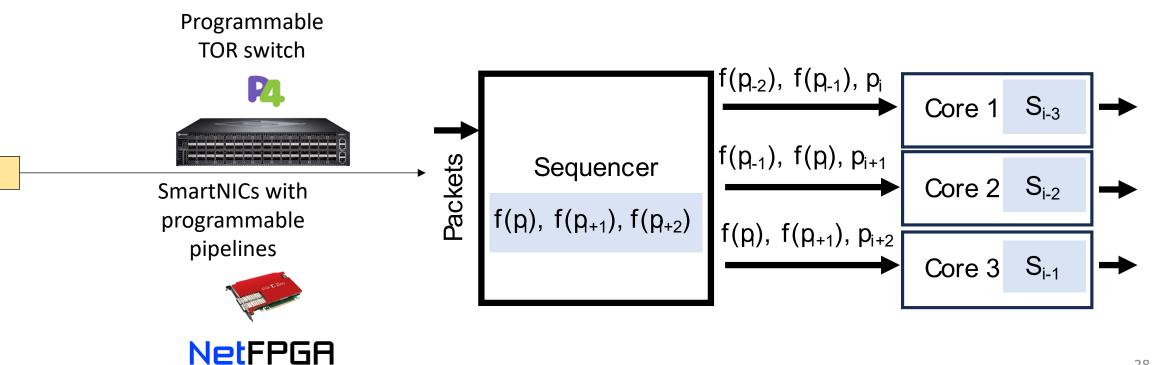
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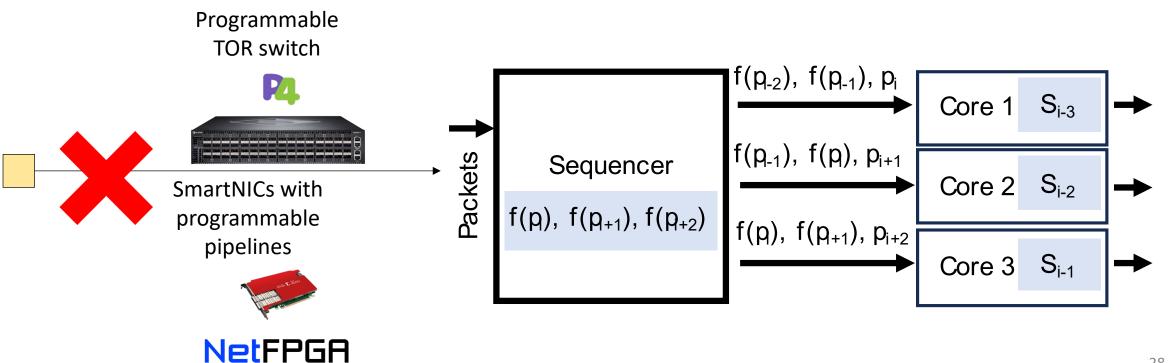




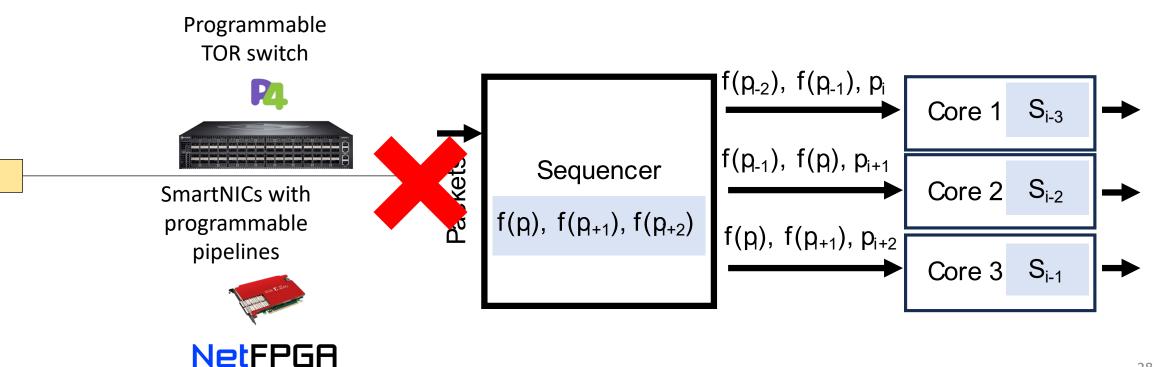
Packets can be lost either



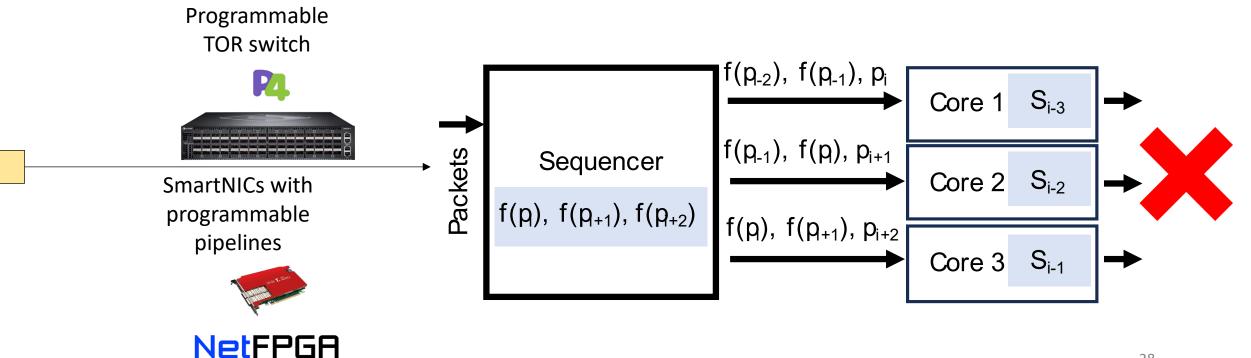
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 - (1) **prior** to the sequencer

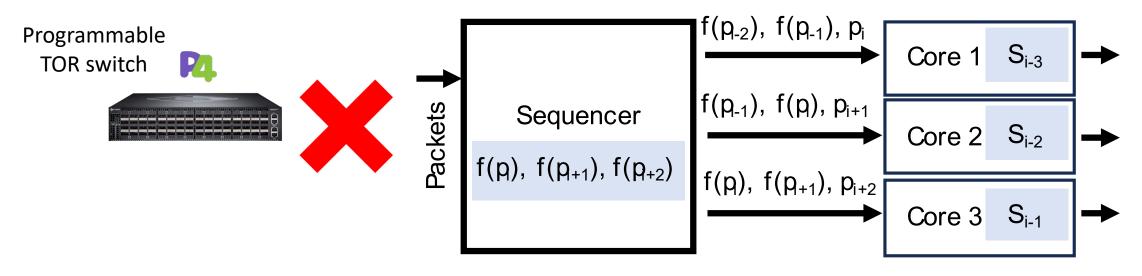


- Packets can be lost either
 - (1) prior to the sequencer
 - (2) after the sequencer but prior to processing at a CPU core

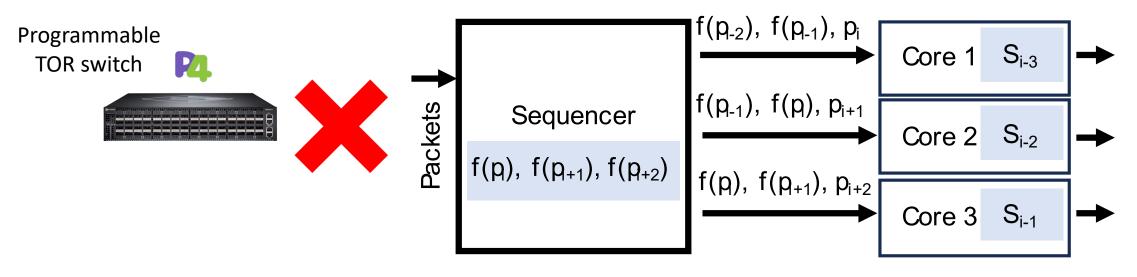


- Packets can be lost either
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 - (2) after the sequencer but prior to processing at a CPU core
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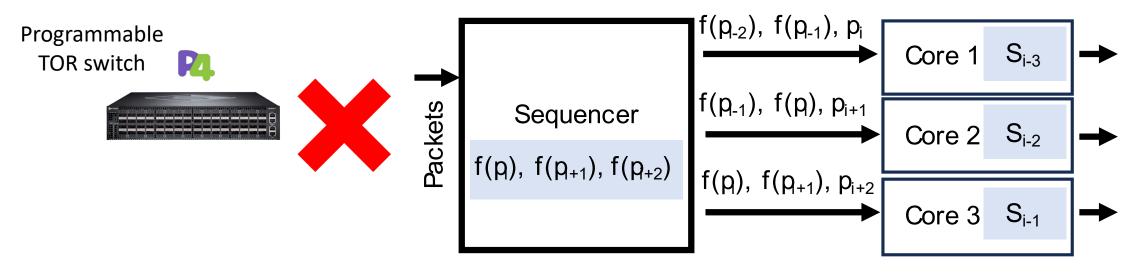




• The only one that represents a problem is (2)



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- Only in the case where the sequence is deployed on a top-of-the-rack switch
 - We can run link-level flow control mechanism like PFC to prevent packet loss between the switch and server cores.



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- ...or it can read the packet history from either the sequencer or a log written by a more up-to-date core
- To achieve this, we:
 - 1. Have the sequence attach an **incrementing sequence number** to each packet
 - 2. Use a per-core, lockless, single-writer multiple-reader log
 - 3. Introduce an algorithm to **catch up the flow state** on each core upon detection of loss

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- Applications using SCR need to be modified to replicate the program state and keep private copies per core
 - A **compiler** can do it automatically!
- Our experiment show that SCR can scale total packet processing throughput linearly with cores, deterministically and independent of flow size distribution